Model Name: 965P-S3

Revision 1.02

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01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	POWER MAP
05	P4_LGA775_A
06	P4_LGA775_B
07	P4_LGA775_C
08	P4_LGA775_D
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10	GMCH-BROADWATER_DDRII
11	GMCH-BROADWATER_PCI E, DMI
12	GMCH-BROADWATER_INT VGA
13	GMCH-BROADWATER_GND
14	GMCH-BROADWATER_PWR
15	DDRII CHANNEL A 1,2
16	DDRII CHANNEL B 1,2
17	DDRII TERMINATION
18	PCI EXPRESS*16 SLOT
19	ICH8 PCI, USB, DMI, LAN
20	ICH8 GPIO, CTRL
21	ICH8 SATA, FAN PWM
22	ICH8 VCC, GND
23	CLOCK GEN CK505
24	PCI EXPRESS*1 ,PCI SLOT 1,2
25	ITE8712GB,RESET DRIVE
26	COM,LPT
27	BIOS,CI,HWM,KB/MS

SHEET	TITLE
28	AZALIA ALC883
29	AUDIO JACK
30	VCORE PWM ISL6312
31	DISCRETE POWER
32	ATX POWER
33	IDE RAID IT8212
34	1394 TI TSB43AB23
35	LAN MARVELL 88E8053
36	FAN CONTROL
37	FRONT PANEL,FUSB,FDD

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Title	Cover Sheet	
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Component value change history

Data	Change Item	Reason
1.0A	release	
1.0B	PCB:1.0 CHANGE TO 1.01	
	ADD R1945 8.2K/4	
	ICH_FAN_TACH0與ICH_FAN_TACH1 分開	
	CPU_TEMP 改到I/O TEMP2	
	CPU PWROK R43 / C13 電阻請移除	
	AUDIO FB 改成 30/6/4A/S	
	ADD C31/C32/C33 10P/4 FOR EMI	
	DU1 指定 ISL6312CRZ/QFN48 WW52週	
	DR53/DR55/DR57 750/6 CHANGE TO 200/6	
	DR11 2.7K/4 CHANGE TO 2K/4	
	DEC5~DEC9 820U/2.5V CHANGE TO 560U/2.5V	
	DDRVTT 改成RT9199	
	1_25V_OV1/2 改成S/B	
	ADD VCORE SMD CAP	
	DR29 75K/4/1 FOR OFFSET , DR35=169K/4/1 FOR FS	
	U54 Marvell8056 --> Marvell8053	
	REMOVE R1865 1K/4,REMOVE DR32 41.2K/4,ADD R1840 0/4 FOR C0/ADD C1332/C1392 0.047U/4	
	PCI_BT REMOVE	
	REMOVE R1942 22/6,,REMOVE RR19 0/6 JMICRON 25MHZ 由X'TAL來	
	ADD RX1 25M/20p/30ppm/49US/20/D,ADD RC1/RC2 33P/4/NPO/50V/J,ADD RR20 1M/4	
1.0C	1. PROCHOT R325=8.45K/4/1 , R327=2.43K/4/1	
	2. VTT_GMCH VOLTAGE R1823=12.7K/6/1 , 21824=6.49K/6/1	
1.0D	1. SPDIF-IN CBC50=470P/6	9.PCB:1.02
	2. DL1 REMOVE?	
	3. JMB363 VCC_18V 確認	
	4. 0ohm REMOVE	
	5. U49 ICS588 --> ICS587	
	6. ADD R1944=0/4	
	7. SPDIF-IN MODIFY	
	8. U49 PIN45加粗	

Circuit or PCB layout change for next version

DATE	Change Item	Reason
1.0E	1. RU1 JMB363 --> GBB363	
	2. GSATAII0_1 CHANGE料號	
	3. SRCCLK_3GPIO C1402,C1403 33P/4 REMOVE	
	4. SPI R1850=1K/4 REMOVE	
	5. JMB363替代VCC1.8V RR39~RR42 REMOVE	
	6. EC42,EC170 470uF/16V --> 820uF/2.5V	
1.0F	1. ATX : 11NH4-020024-71R-->11NH4-020024-81R~84R	
	2. U54 88E8053 --> 88E8056	
	3. DR53 200/6 --> 300/6	
	4. PCB ADD 精成,鼎富,大陸智恩.全成信	
	5. LAN RSET LR8 4.87K/4/1 --> 4.64K/4/1	

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Title: BOM & PCB MODIFY HISTORY

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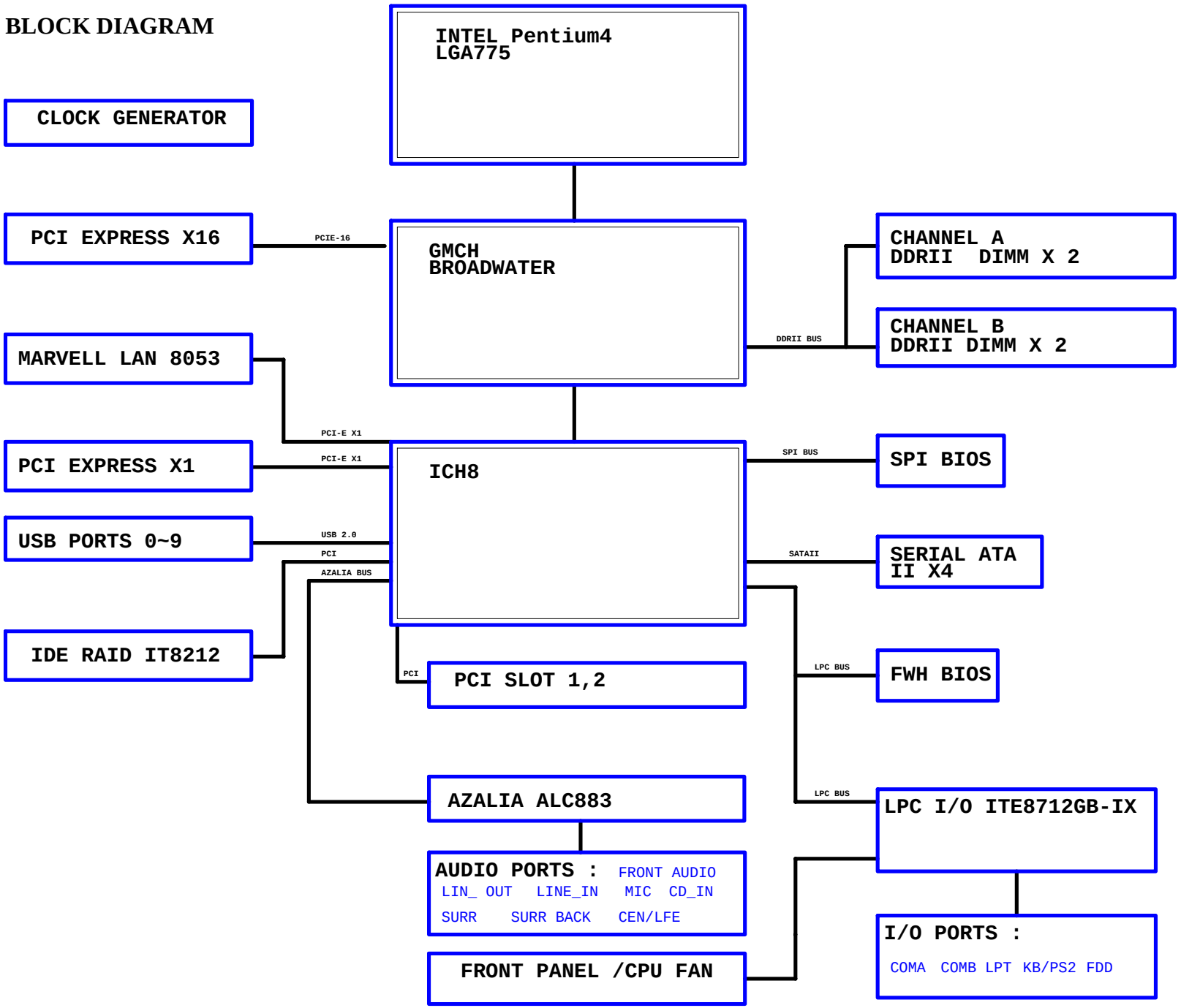
BLOCK DIAGRAM



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Title	BLOCK DIAGRAM	
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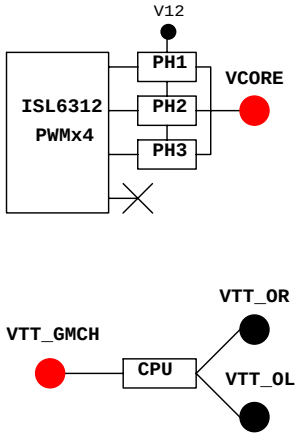
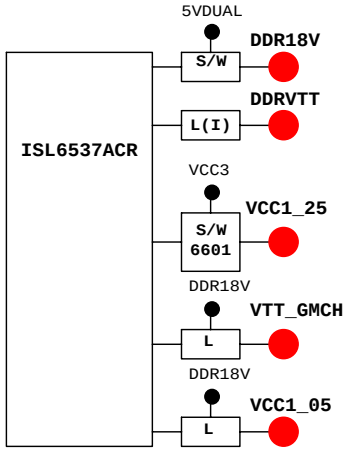
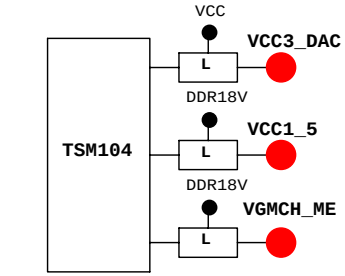
ICH8 GPIO LIST TABLE

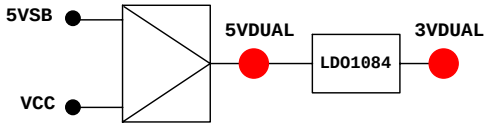
PIN NAME	PWR WELL	AFTER/ PLTRST	USAGE	NOTE
GP0	MAIN	IN	-ACZ_DET	P/U 8.2K VCC3
GP1/TACH1	MAIN	IN	ICH_FAN_TACH1	P/U 8.2K VCC3
GP2/PIRQE#	MAIN	IN	-PIRQE	P/U 8.2K VCC3
GP3/PIRQF#	MAIN	IN	-PIRQF	P/U 8.2K VCC3
GP4/PIRQG#	MAIN	IN	-PIRQG	P/U 8.2K VCC3
GP5/PIRQH#	MAIN	IN	-PIRQH	P/U 8.2K VCC3
GP6/TACH2	MAIN	IN	ICH_FAN_TACH2	P/U 8.2K VCC3
GP7/TACH3	MAIN	IN	ICH_FAN_TACH3	P/U 8.2K VCC3
GP8	STBY	IN	GPIO8(DUALBIOS_INPUT)	P/U 8.2K 3VDUAL
GP9	STBY	OUT	WOL_ONLY	P/D 100K GND
GP10	STBY	IN	CLGPIO1	P/U 8.2K 3VDUAL
GP11/SMBALERT#	STBY	OUT	-SMBALRT	P/U 8.2K 3VDUAL
GP12	STBY	IN	MB_ID0	P/U 8.2K 3VDUAL
GP13	STBY	IN	-LPCPME	P/U 8.2K 3VDUAL
GP14	STBY	IN	CLGPIO2	P/U 8.2K 3VDUAL
GP15	STBY	OUT	LAN_DISABLE(STP_PCI-)	N/A
GP16	MAIN	OUT/LOW	RESET	N/A
GP17/TACH0	MAIN	IN	ICH_FAN_TACH0	P/U 8.2K VCC3
GP18	MAIN	OUT	MB_ID1	P/U 8.2K VCC3
GP19	MAIN	IN	SATA1GP	P/U 8.2K VCC3
GP20	MAIN	OUT	-SPI_WP0	P/U 1K 3VCL
GP21	MAIN	IN	SATA0GP	P/U 8.2K VCC3
GP22	MAIN	IN	SCLOCK	P/U 8.2K VCC3
GP23	MAIN	OUT	-LDRQ1	P/U 8.2K VCC3
GP24	STBY	OUT	CLGPIO0	P/U 8.2K 3VDUAL
GP25	STBY	IN	MB_ID2(STP_CPU-)	P/U 8.2K 3VDUAL
GP26/S4_STATE#	STBY	OUT	S4_STATE#	P/U 8.2K 3VDUAL
GP27	STBY	OUT/LOW	GPIO27(EL_STATE0)	P/U 8.2K 3VDUAL
GP28	STBY	OUT/LOW	PWR_LED(EL_STATE1)	N/A
GP29/OC5#	STBY	IN	-USBOC_R	P/U FUSEVCC
GP30/OC6#	STBY	IN	-USBOC_R	P/U FUSEVCC
GP31/OC7#	STBY	IN	-USBOC_R	P/U FUSEVCC
GP32	MAIN	OUT	DUAL_BIOS	P/U 100K+1M VCC3
GP33	MAIN	OUT	DUAL_BIOS	P/U 8.2K VCC3
GP34	MAIN	OUT/LOW	GPIO34/SMB_RST	N/A
GP35	MAIN	OUT	SATACLKREQ#	N/A
GP36	MAIN	IN	SATA2GP	P/U 8.2K VCC3
GP37	MAIN	IN	SATA3GP	P/U 8.2K VCC3
GP38	MAIN	IN	SLOAD	P/U 8.2K VCC3
GP39	MAIN	IN	GPIO39	P/D 8.2K GND
GP48	MAIN	IN	GPIO48	P/U 8.2K VCC3
GP49	MAIN	IN	CPUPWROK	P/U 100 VTT_OL

VCORE:3 PHASE PWM--ISL6312









Gigabyte Technology		
Title: TABLE LIST		
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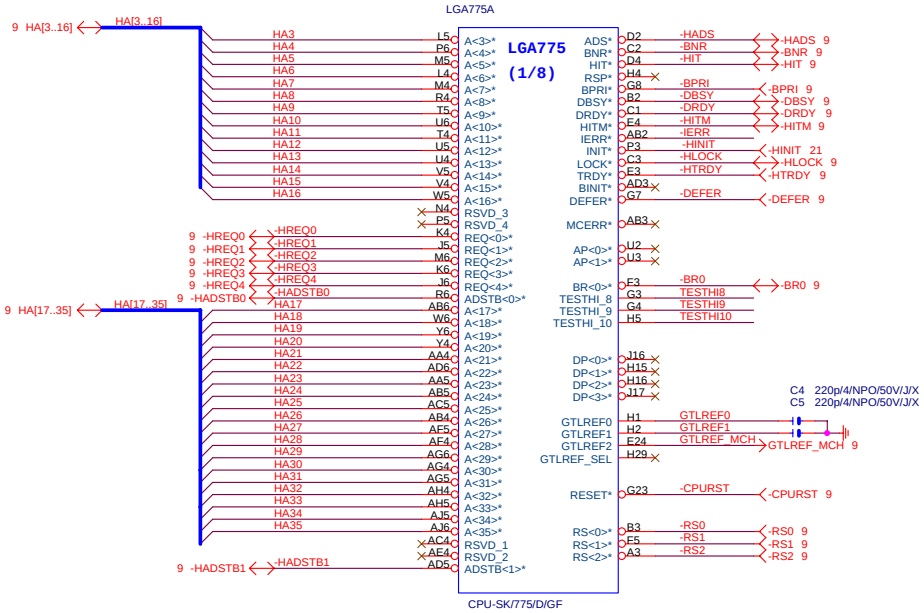
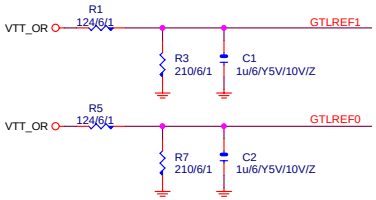
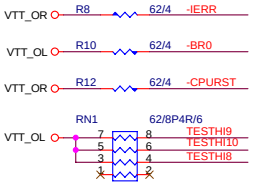
HA/REQ:4/14

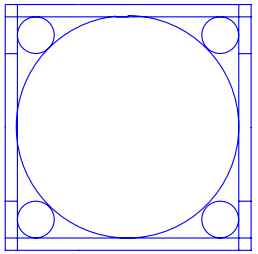
ADSTB:4/17



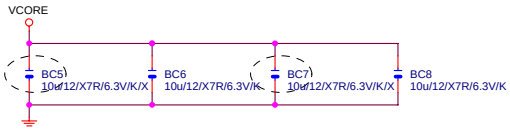


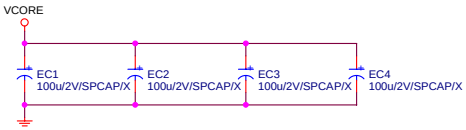


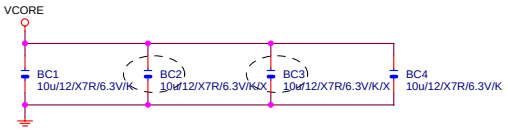
CR
CPU RETAINTION/X



Impedance=50 +- 15% for 4 -layer







Gigabyte Technology			
Title: P4_LGA775-A			
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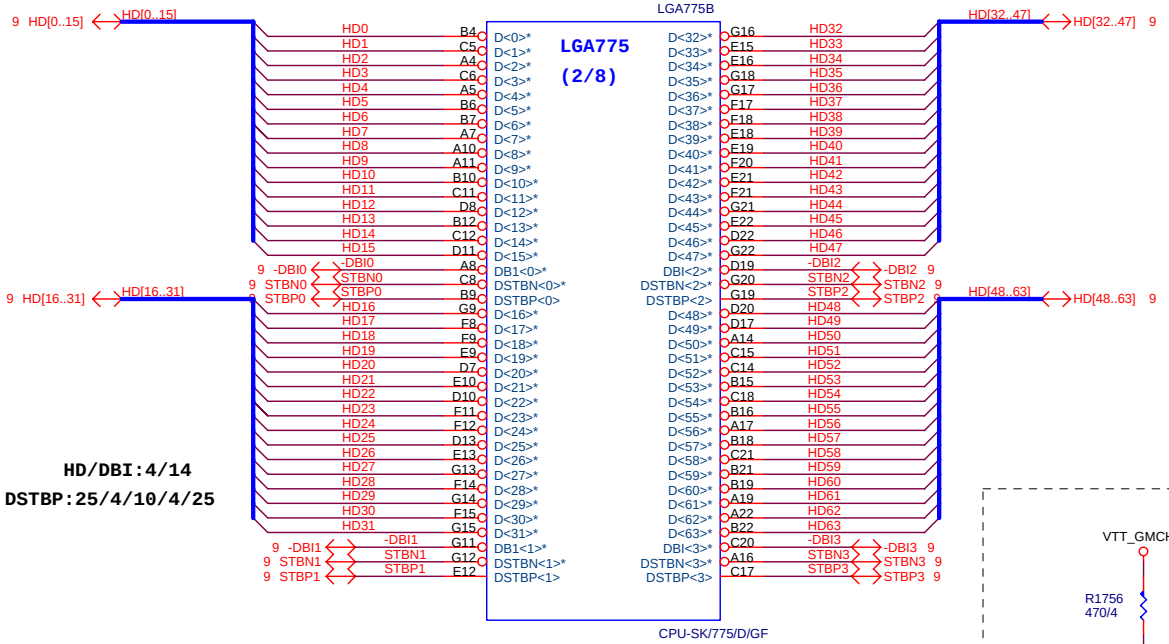

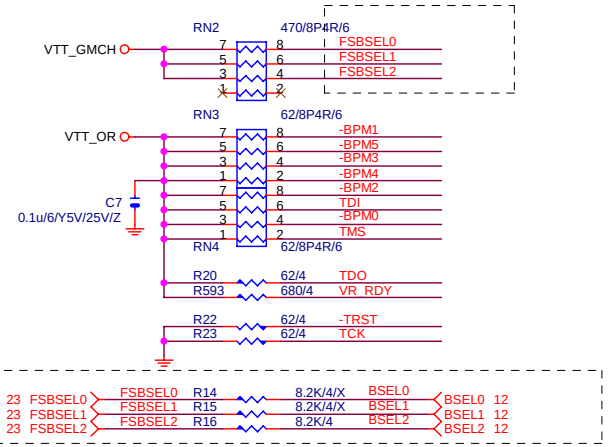

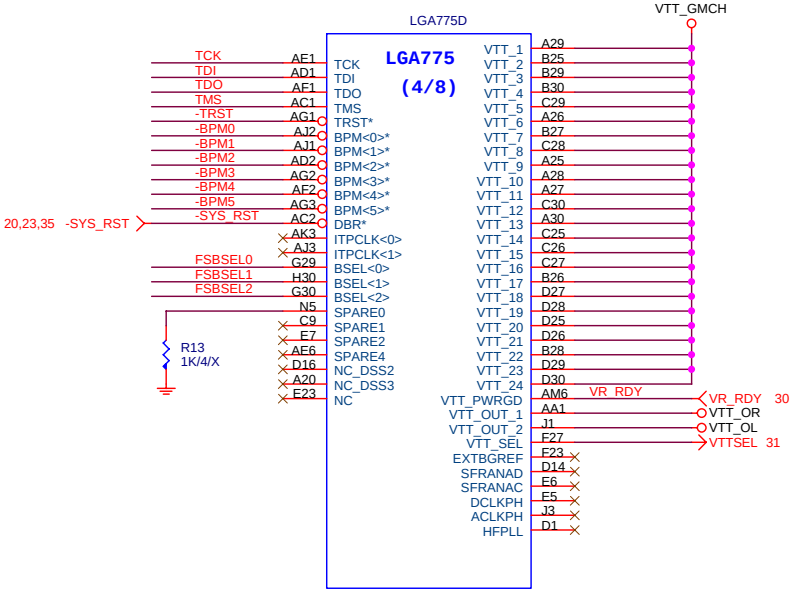

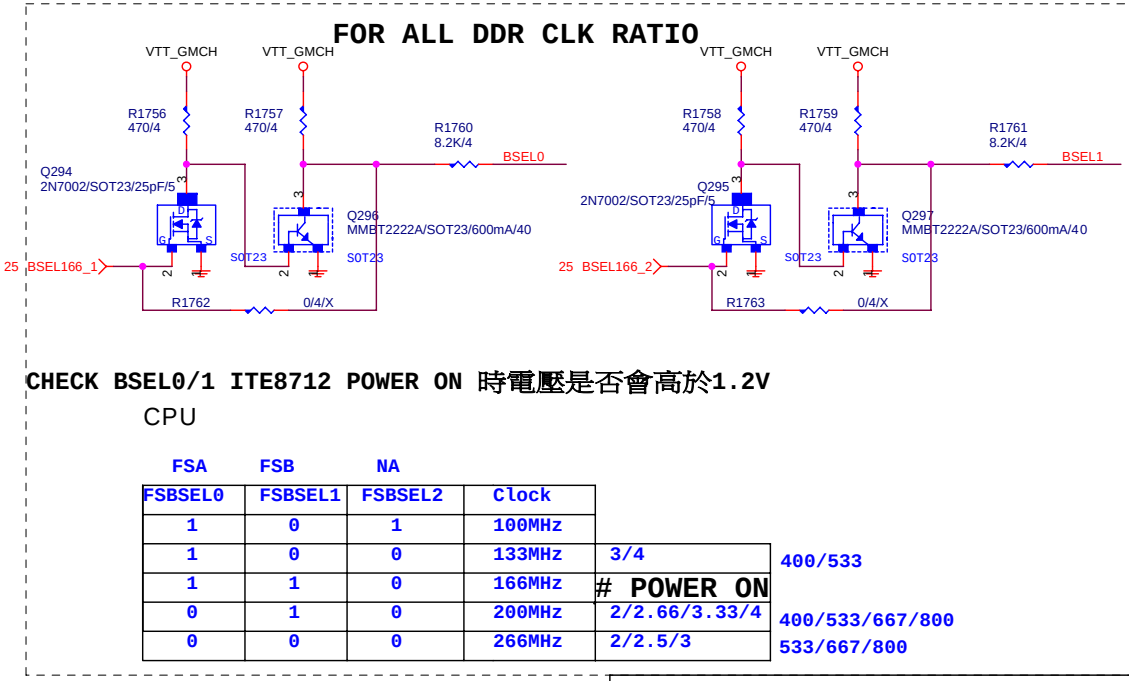

CHECK BSEL0/1 ITE8712 POWER ON 時電壓是否會高於1.2V

CPU

FSA	FSB	NA		
FSBSEL0	FSBSEL1	FSBSEL2	Clock	
1	0	1	100MHz	
1	0	0	133MHz	3/4
1	1	0	166MHz	# POWER ON
0	1	0	200MHz	2/2.66/3.33/4
0	0	0	266MHz	2/2.5/3

400/533

400/533/667/800

533/667/800

Gigabyte Technology

Title	P4_LGA775-B,D	
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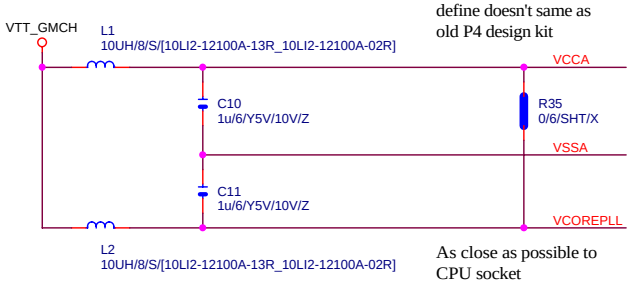
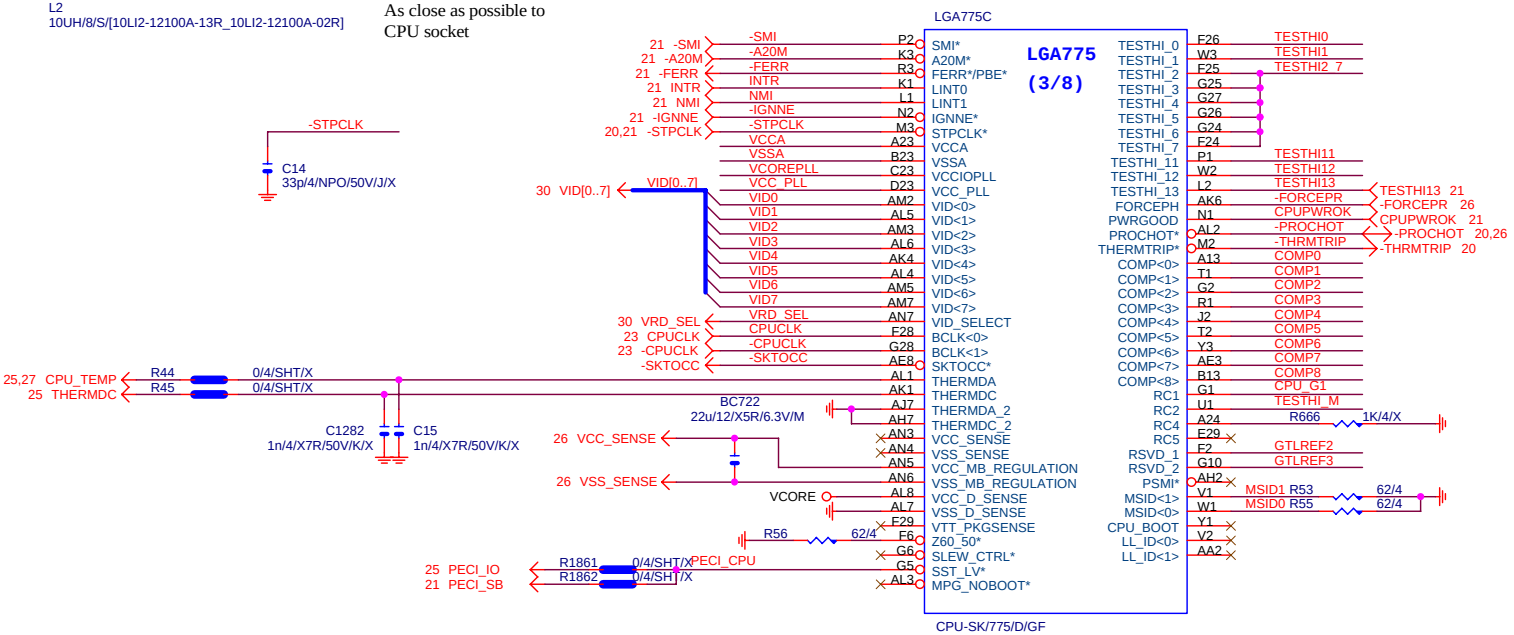
Note:

VCCA & VCOREPLL define doesn't same as old P4 design kit

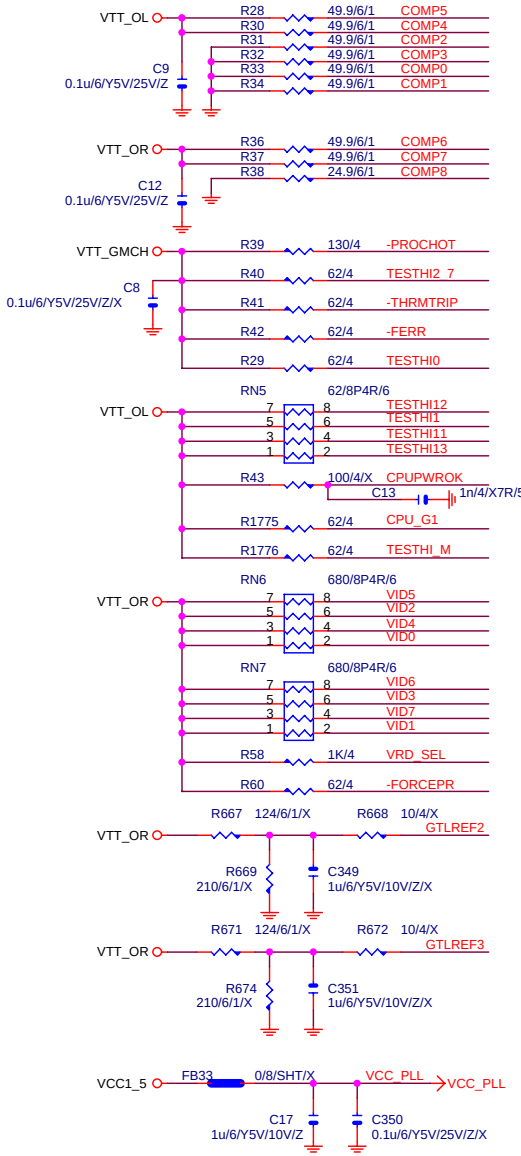
Trace width doesn't less than 12 Mil

As close as possible to CPU socket





Place outside of CPU socket



PECI:Platform Environment Control Interface

Gigabyte Technology			
Title: P4_LGA775-C			
Size: B	Document Number: 965P-S3		Rev: 1.02
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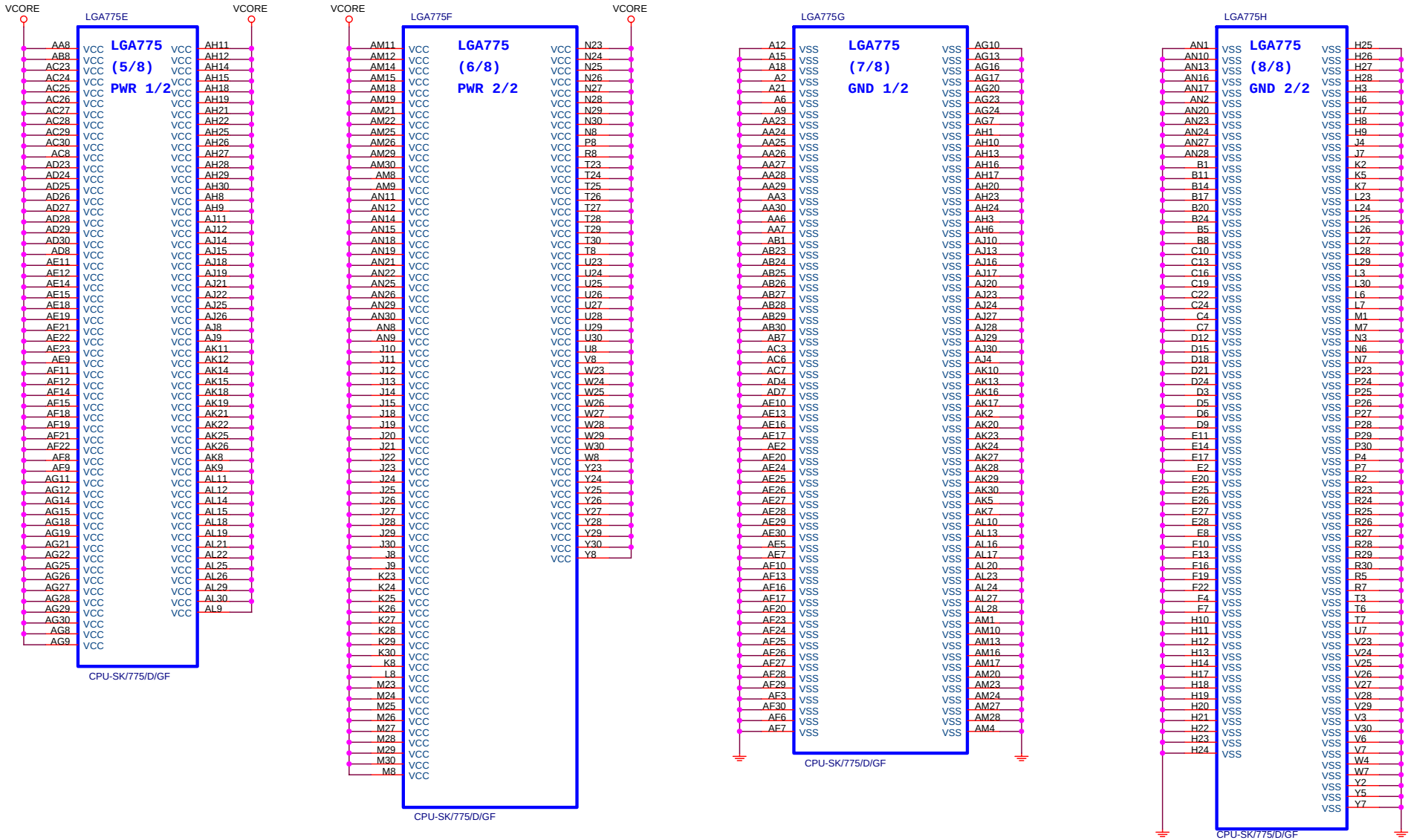

Gigabyte Technology			
Title	P4_LGA775-E,F,G,H		
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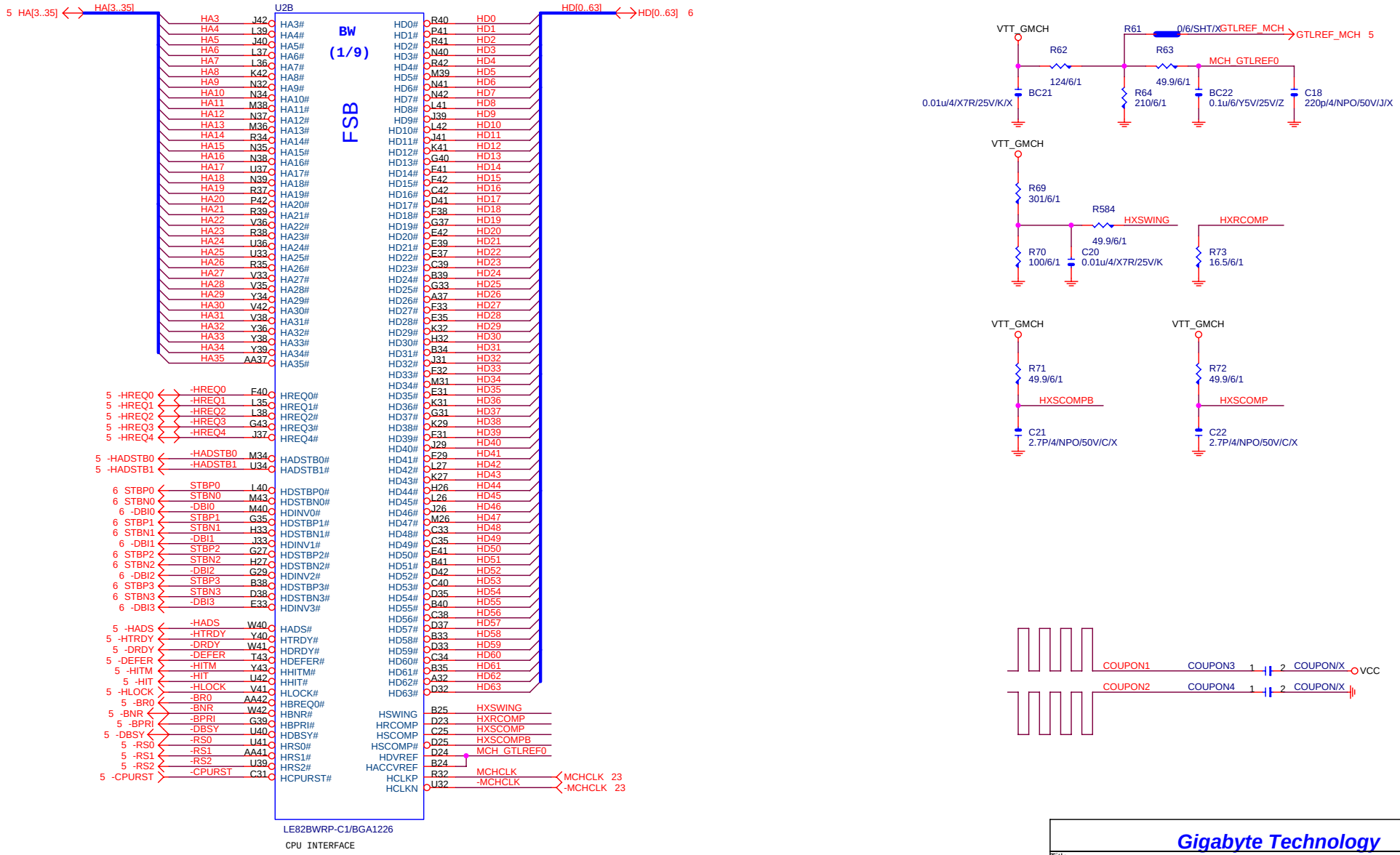

Gigabyte Technology		
Title: GMCH-HOST		
Size: B	Document Number: 965P-S3	Rev: 1.02
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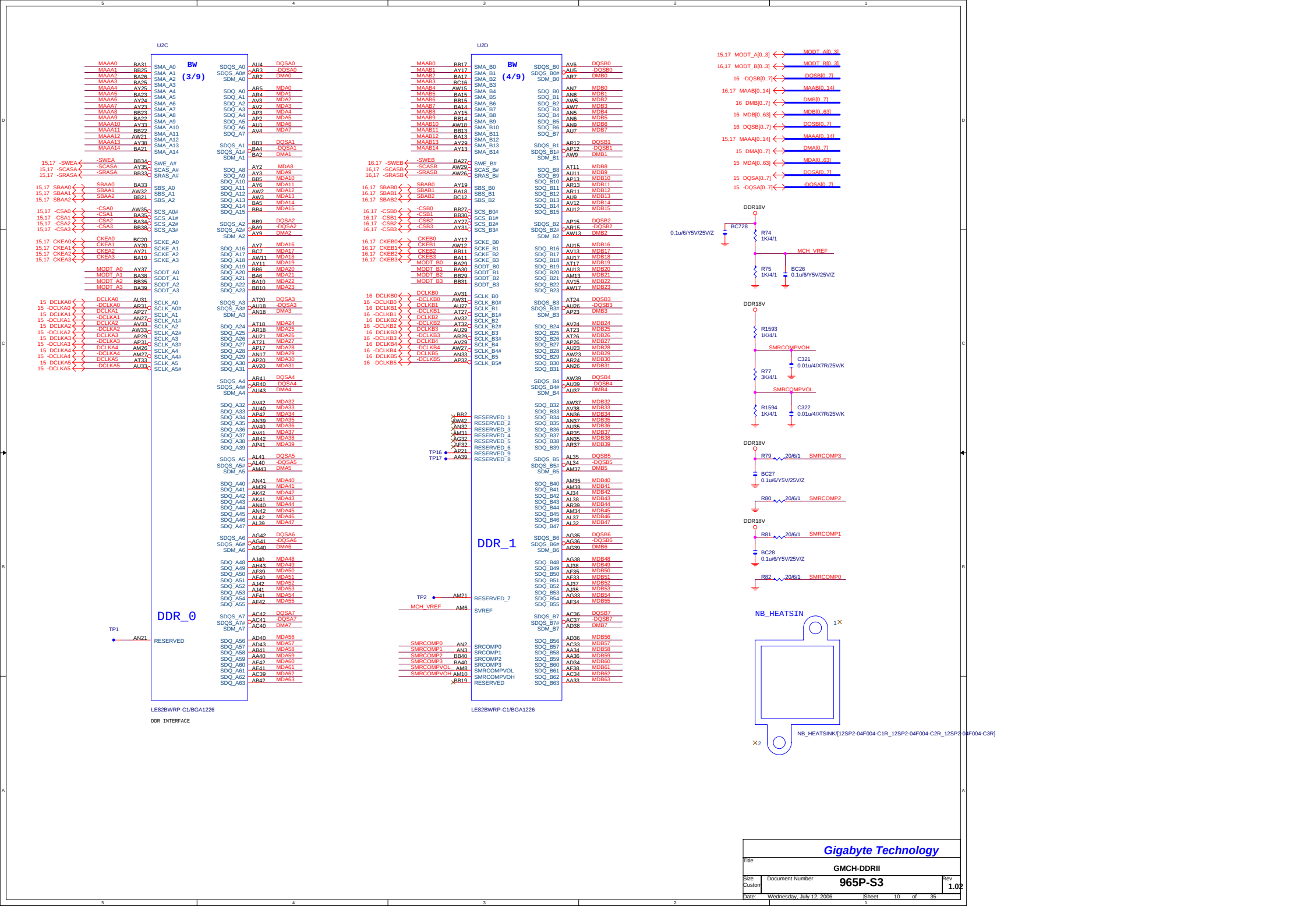
U2C
BW (3/9)
DDR_0
LE82BWRP-C1/BGA1226
DDR INTERFACE
U2D
BW (4/9)
DDR_1
LE82BWRP-C1/BGA1226
DDR18V
MCH_VREF
SMRCOMPVOH
SMRCOMPVOL
NB_HEATSIN
NB_HEATSINK/[12SP2-04F004-C1R_12SP2-04F004-C2R_12SP2-04F004-C3R]
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GMCH-DDRII
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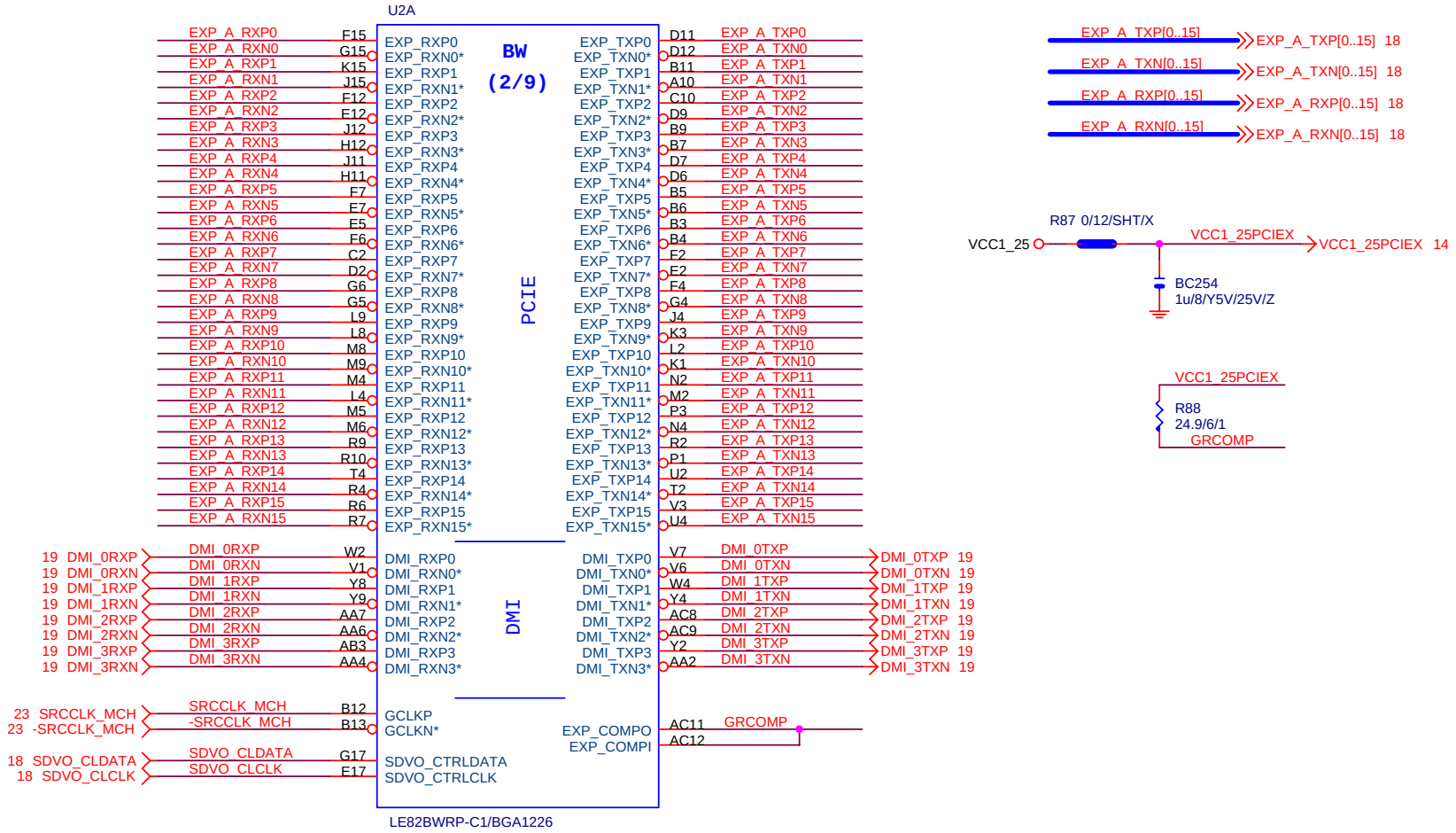

Gigabyte Technology		
Title: GMCH-PCI E & DMI		
Size: Custom	Document Number: 965P-S3	Rev: 1.02
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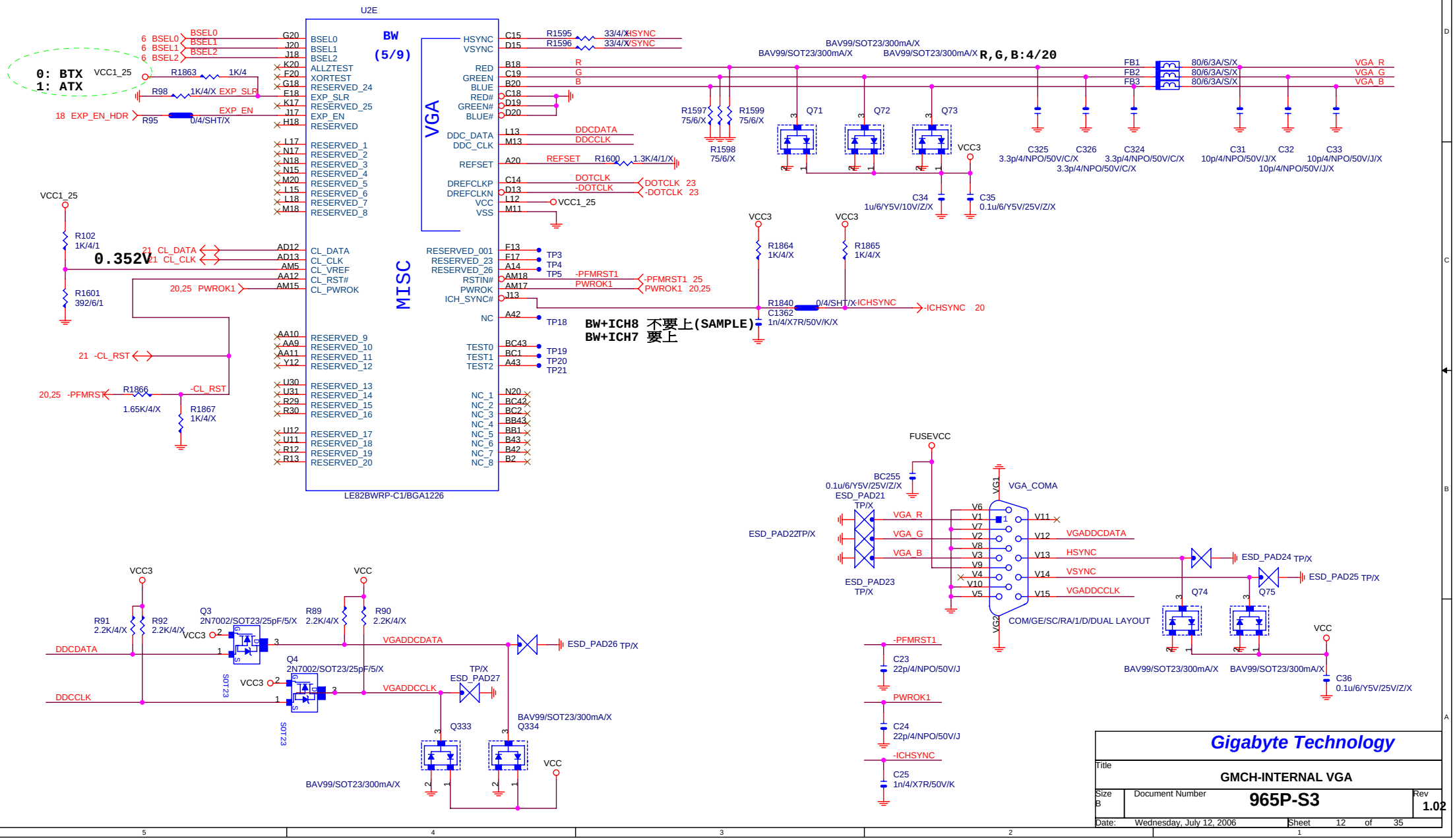
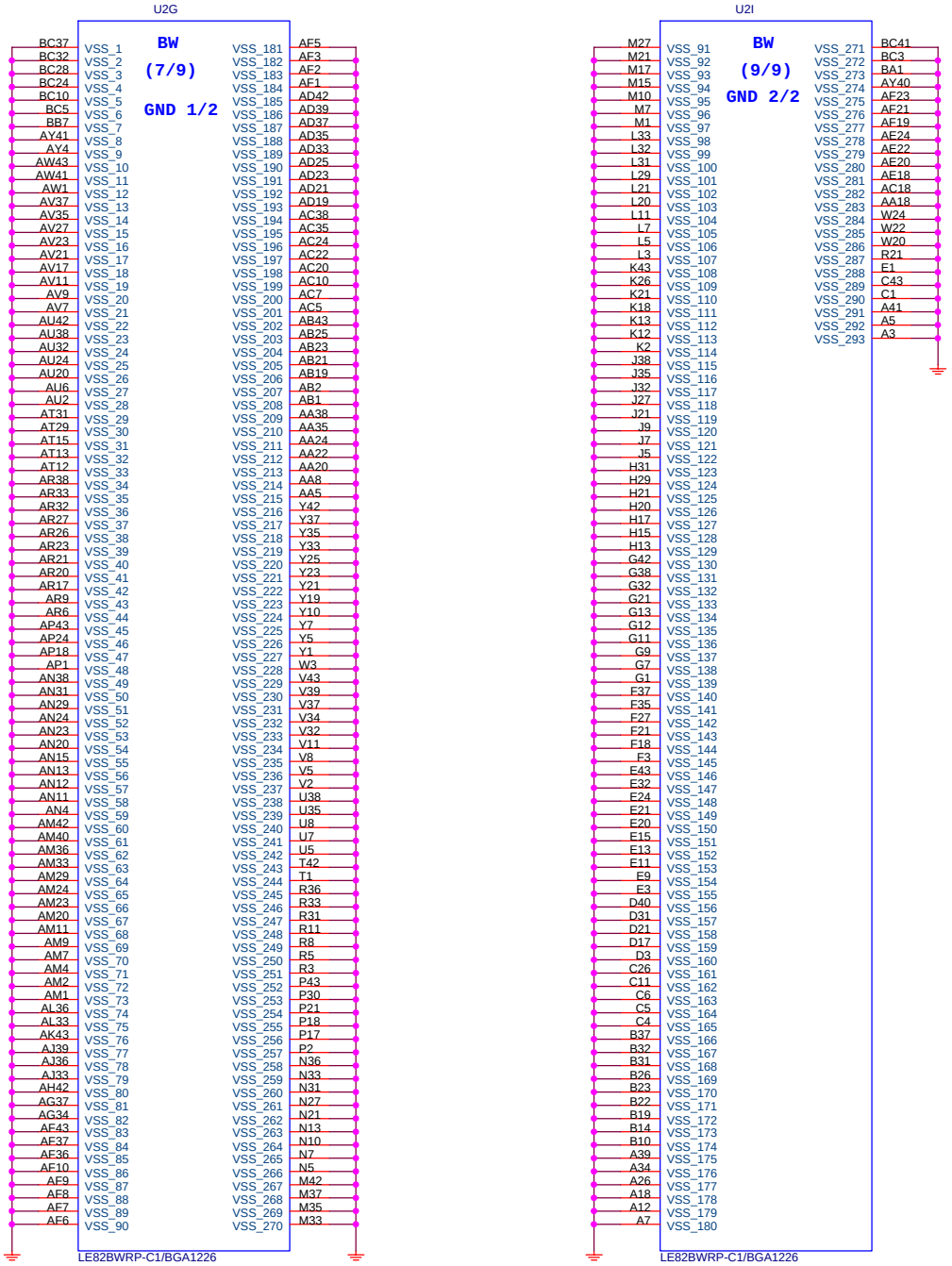


Gigabyte Technology		
Title: GMCH-INTERNAL VGA		
Size: B	Document Number: 965P-S3	Rev: 1.02
Date: Wednesday, July 12, 2006	Sheet 12 of 35	



Gigabyte Technology

Title	GMCH-GND		
Size: Custom	Document Number: 965P-S3		Rev: 1.02
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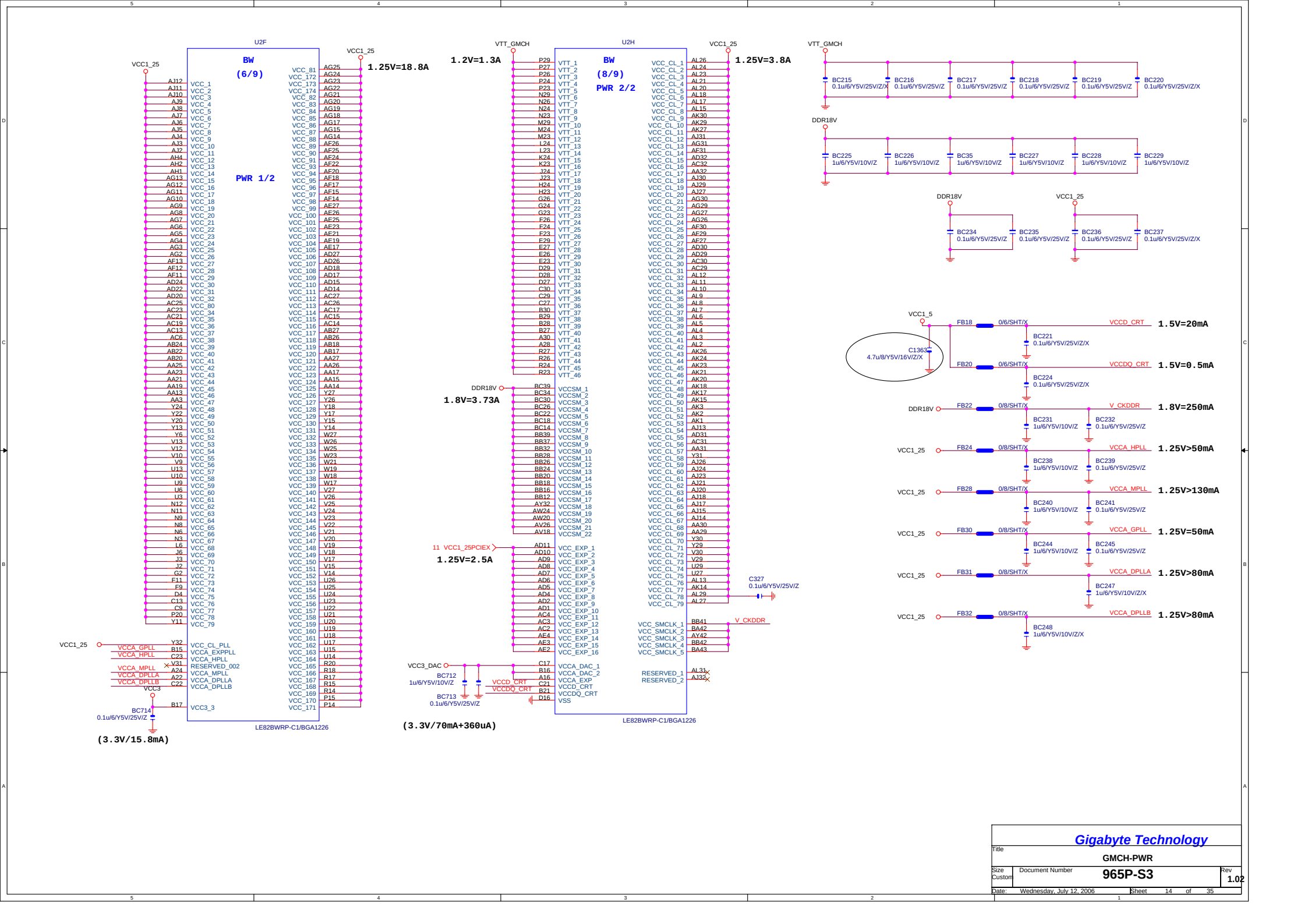
U2F
BW
(6/9)
PWR 1/2
VCC1_25
1.25V=18.8A
(3.3V/15.8mA)
LE82BWRP-C1/BGA1226
U2H
BW
(8/9)
PWR 2/2
VTT_GMCH
1.2V=1.3A
DDR18V
1.8V=3.73A
11 VCC1_25PCIEX
1.25V=2.5A
VCC3_DAC
(3.3V/70mA+360uA)
LE82BWRP-C1/BGA1226
1.25V=3.8A
C327
0.1u/6Y5V/25V/Z
V_CKDDR
BC714
0.1u/6Y5V/25V/Z
BC712
1u/6Y5V/10V/Z
BC713
0.1u/6Y5V/25V/Z
BC215
0.1u/6Y5V/25V/Z/X
BC216
0.1u/6Y5V/25V/Z
BC217
0.1u/6Y5V/25V/Z
BC218
0.1u/6Y5V/25V/Z
BC219
0.1u/6Y5V/25V/Z
BC220
0.1u/6Y5V/25V/Z/X
BC225
1u/6Y5V/10V/Z
BC226
1u/6Y5V/10V/Z
BC35
1u/6Y5V/10V/Z
BC227
1u/6Y5V/10V/Z
BC228
1u/6Y5V/10V/Z
BC229
1u/6Y5V/10V/Z
BC234
0.1u/6Y5V/25V/Z
BC235
0.1u/6Y5V/25V/Z
BC236
0.1u/6Y5V/25V/Z
BC237
0.1u/6Y5V/25V/Z/X
VCC1_5
C1363
4.7u/8Y5V/16V/Z/X
FB18
0/6/SHT/X
VCCD_CRT
1.5V=20mA
BC221
0.1u/6Y5V/25V/Z/X
FB20
0/6/SHT/X
VCCDQ_CRT
1.5V=0.5mA
BC224
0.1u/6Y5V/25V/Z/X
FB22
0/8/SHT/X
V_CKDDR
1.8V=250mA
BC231
1u/6Y5V/10V/Z
BC232
0.1u/6Y5V/25V/Z
FB24
0/8/SHT/X
VCCA_HPLL
1.25V>50mA
BC238
1u/6Y5V/10V/Z
BC239
0.1u/6Y5V/25V/Z
FB28
0/8/SHT/X
VCCA_MPLL
1.25V>130mA
BC240
1u/6Y5V/10V/Z
BC241
0.1u/6Y5V/25V/Z
FB30
0/8/SHT/X
VCCA_GPLL
1.25V=50mA
BC244
1u/6Y5V/10V/Z
BC245
0.1u/6Y5V/25V/Z
FB31
0/8/SHT/X
VCCA_DPLLA
1.25V>80mA
BC247
1u/6Y5V/10V/Z/X
FB32
0/8/SHT/X
VCCA_DPLLB
1.25V>80mA
BC248
1u/6Y5V/10V/Z/X
Gigabyte Technology
Title
GMCH-PWR
Size
Custom
Document Number
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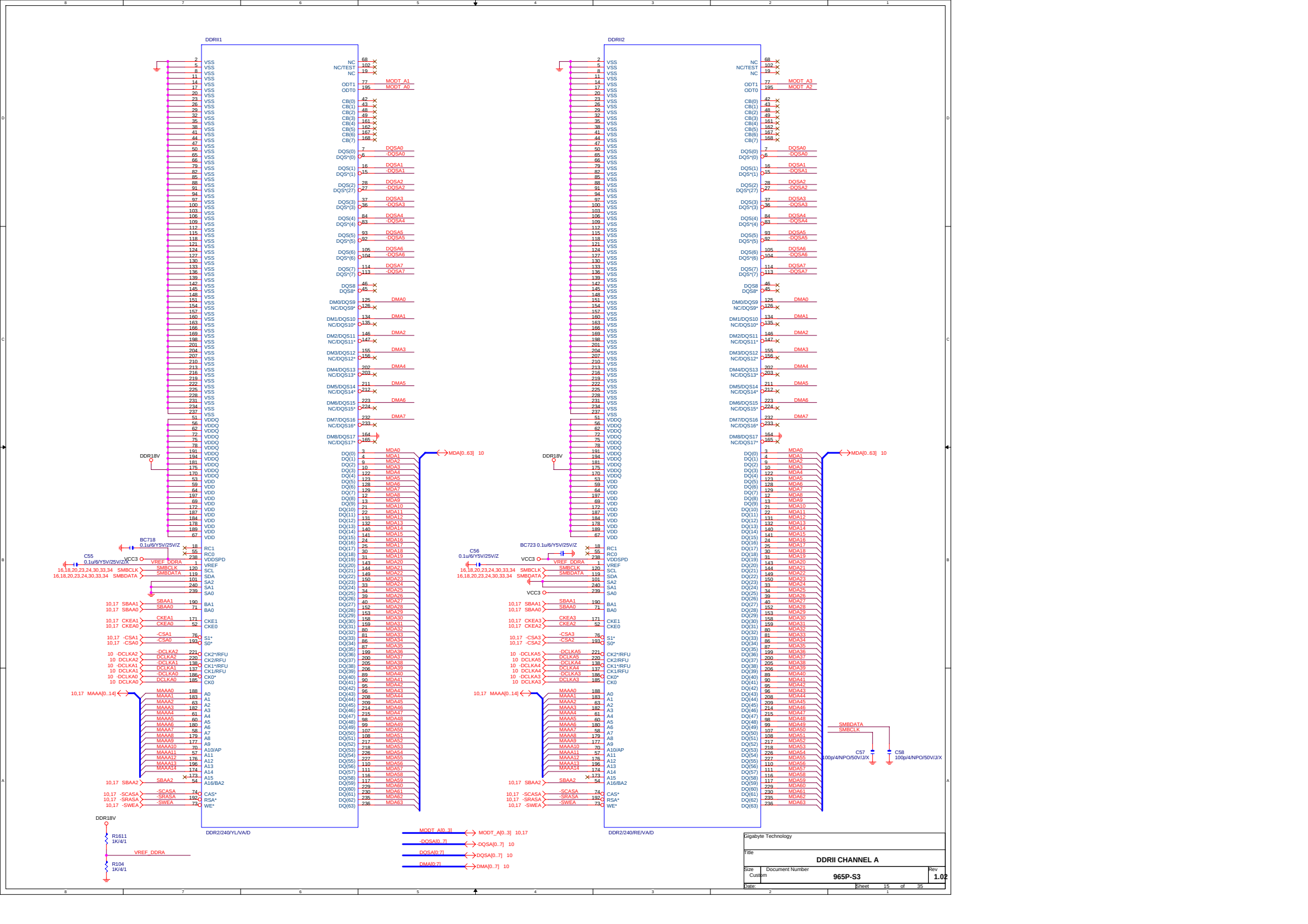
35



Gigabyte Technology		
Title	DDRII CHANNEL A	
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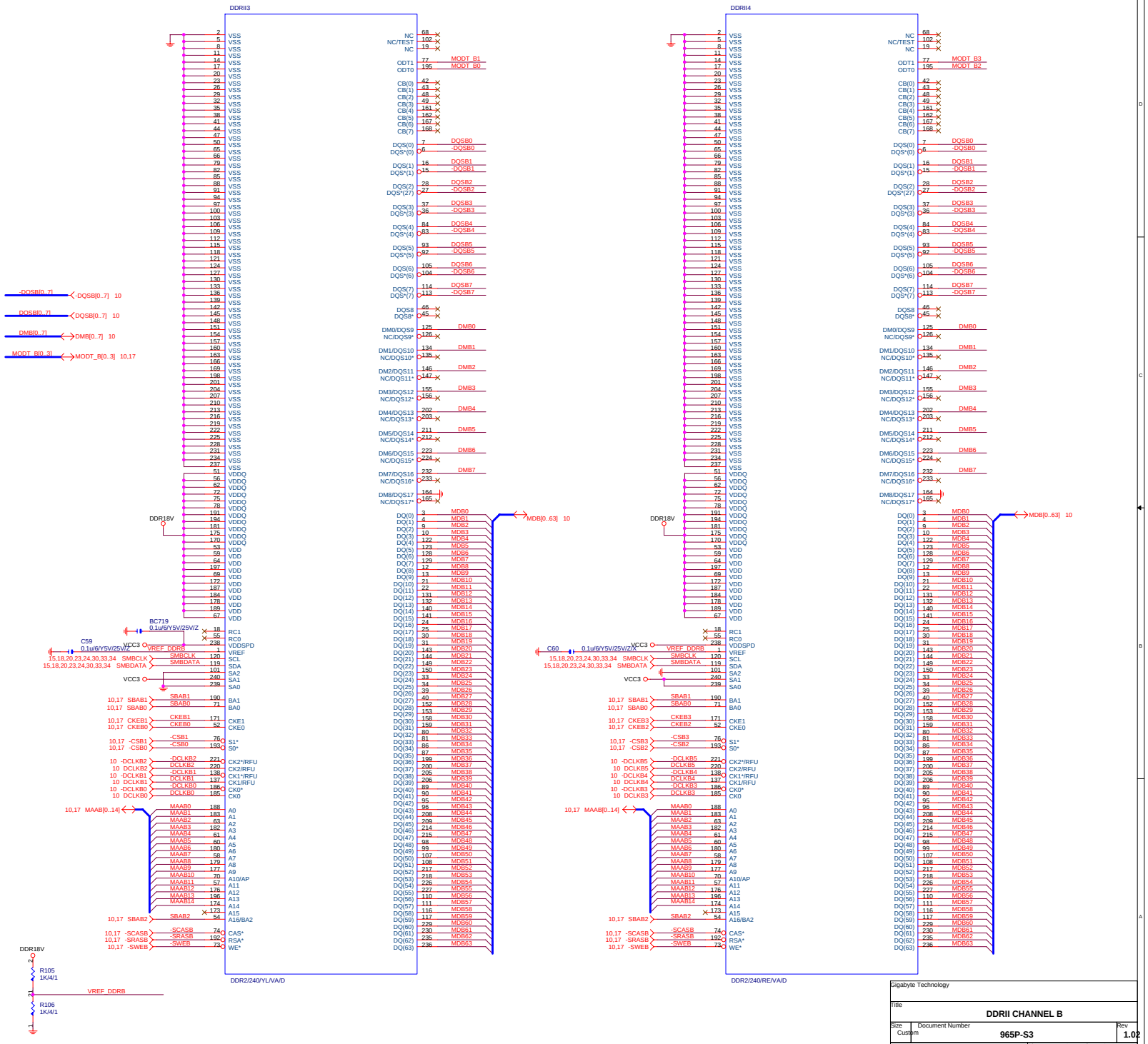

Gigabyte Technology	
Title	DDRII CHANNEL B
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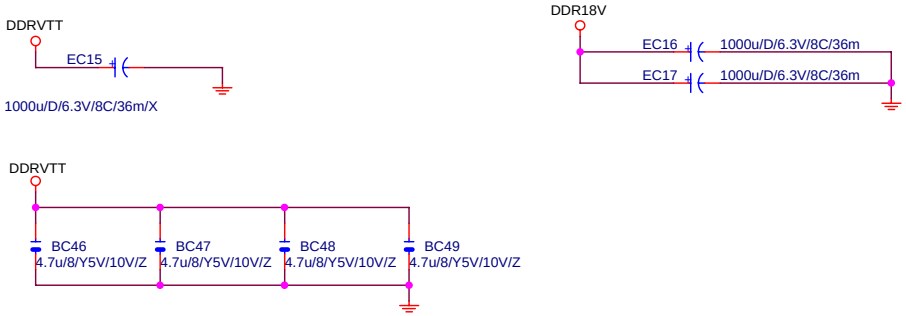
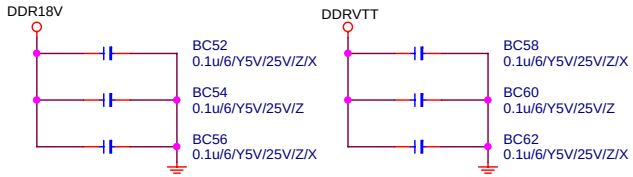
DDR TERMINATION CHANNEL A

DDRVTT Decouple



DDR18V Decouple

DDRVTT Decouple



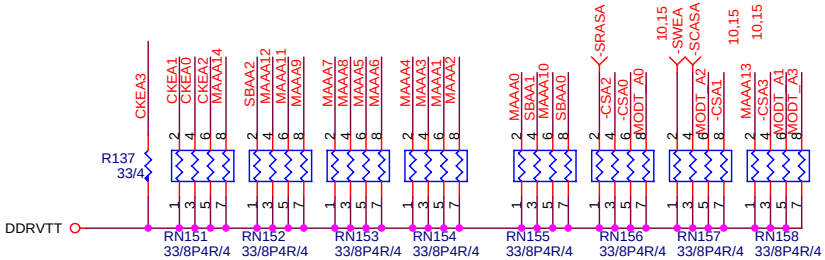
SBAA[0..2] SBAA[0..2] 10,15

-CSA[0..3] -CSA[0..3] 10,15

CKEA[0..3] CKEA[0..3] 10,15

MAAA[0..14] MAAA[0..14] 10,15

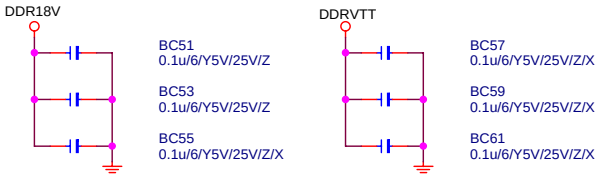
MODT_A[0..3] MODT_A[0..3] 10,15



DDR TERMINATION CHANNEL B

DDR18V Decouple

DDRVTT Decouple



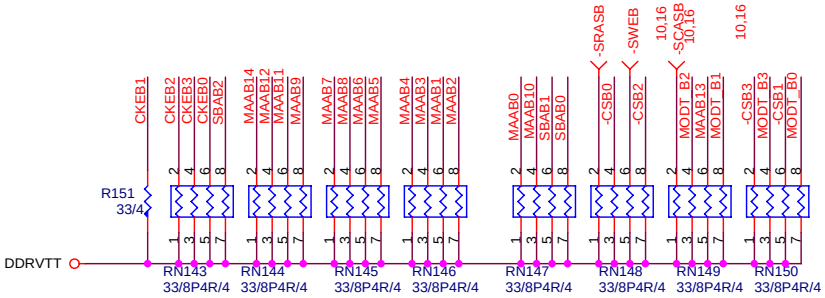
MODT_B[0..3] MODT_B[0..3] 10,16

SBAB[0..2] SBAB[0..2] 10,16

-CSB[0..3] -CSB[0..3] 10,16

CKEB[0..3] CKEB[0..3] 10,16

MAAB[0..14] MAAB[0..14] 10,16



Gigabyte Technology

Title: DDRII TERMINATOR

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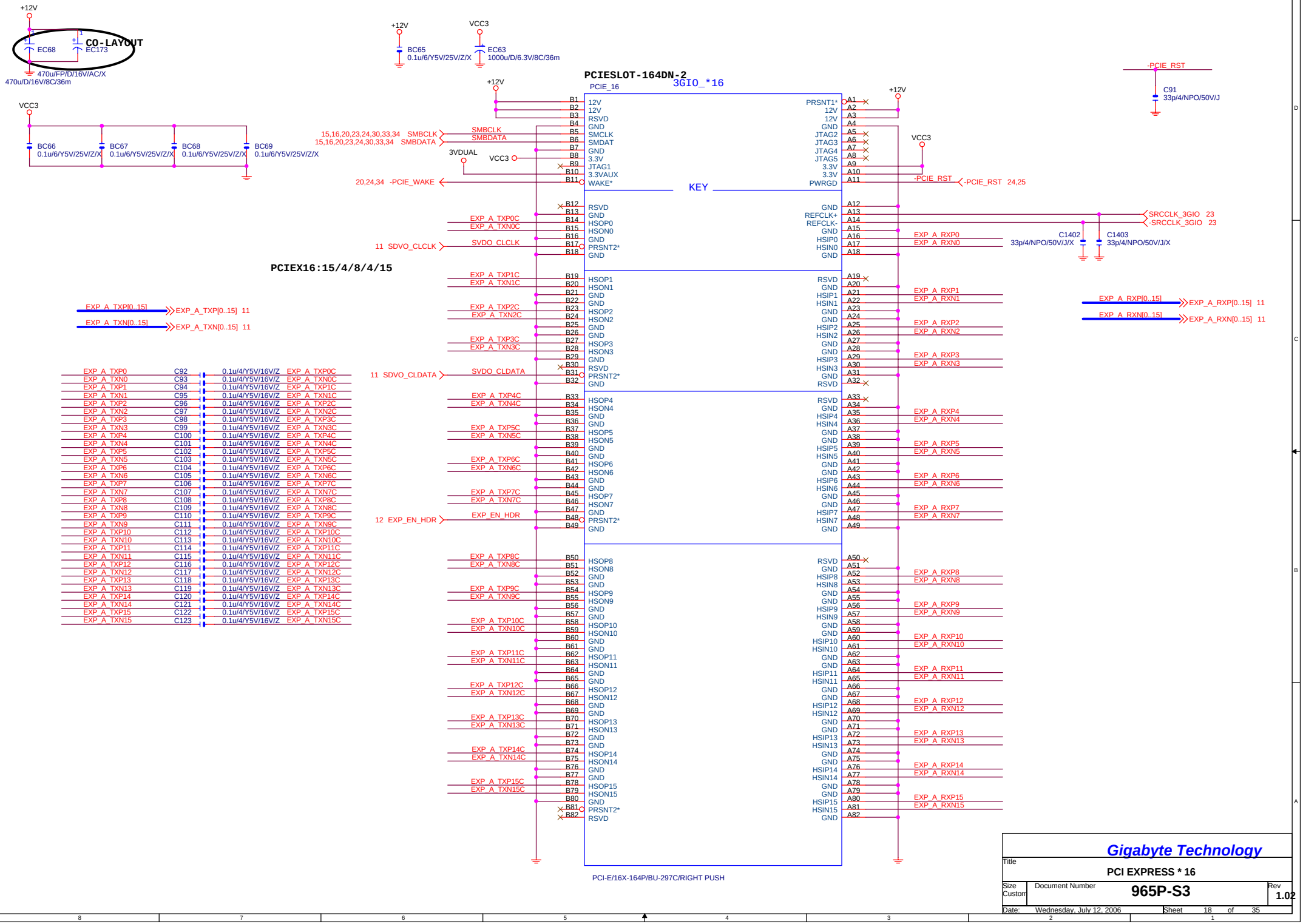
+12V
EC68
EC173
C0-LAYOUT
470u/FP/D/16V/AC/X
470u/D/16V/8C/36m
VCC3
BC66
0.1u/6/Y5V/25V/Z/X
BC67
0.1u/6/Y5V/25V/Z/X
BC68
0.1u/6/Y5V/25V/Z/X
BC69
0.1u/6/Y5V/25V/Z/X
+12V
BC65
0.1u/6/Y5V/25V/Z/X
VCC3
EC63
1000u/D/6.3V/8C/36m
PCIESLOT-164DN-2
PCIE_16
3GIO_*16
KEY
PCIEX16:15/4/8/4/15
15,16,20,23,24,30,33,34 SMBCLK
15,16,20,23,24,30,33,34 SMBDATA
SMBCLK
SMBDATA
3VDUAL
VCC3
20,24,34 -PCIE_WAKE
11 SDVO_CLCLK
SDVO_CLCLK
11 SDVO_CLDATA
SDVO_CLDATA
12 EXP_EN_HDR
EXP_EN_HDR
-PCIE_RST
C91
33p/4/NPO/50V/J
-PCIE_RST 24,25
SRCCLK_3GIO 23
-SRCCLK_3GIO 23
C1402
33p/4/NPO/50V/J/X
C1403
33p/4/NPO/50V/J/X
EXP_A_TXP[0..15]
EXP_A_TXP[0..15] 11
EXP_A_TXN[0..15]
EXP_A_TXN[0..15] 11
EXP_A_RXP[0..15]
EXP_A_RXP[0..15] 11
EXP_A_RXN[0..15]
EXP_A_RXN[0..15] 11
PCI-E/16X-164P/BU-297C/RIGHT PUSH
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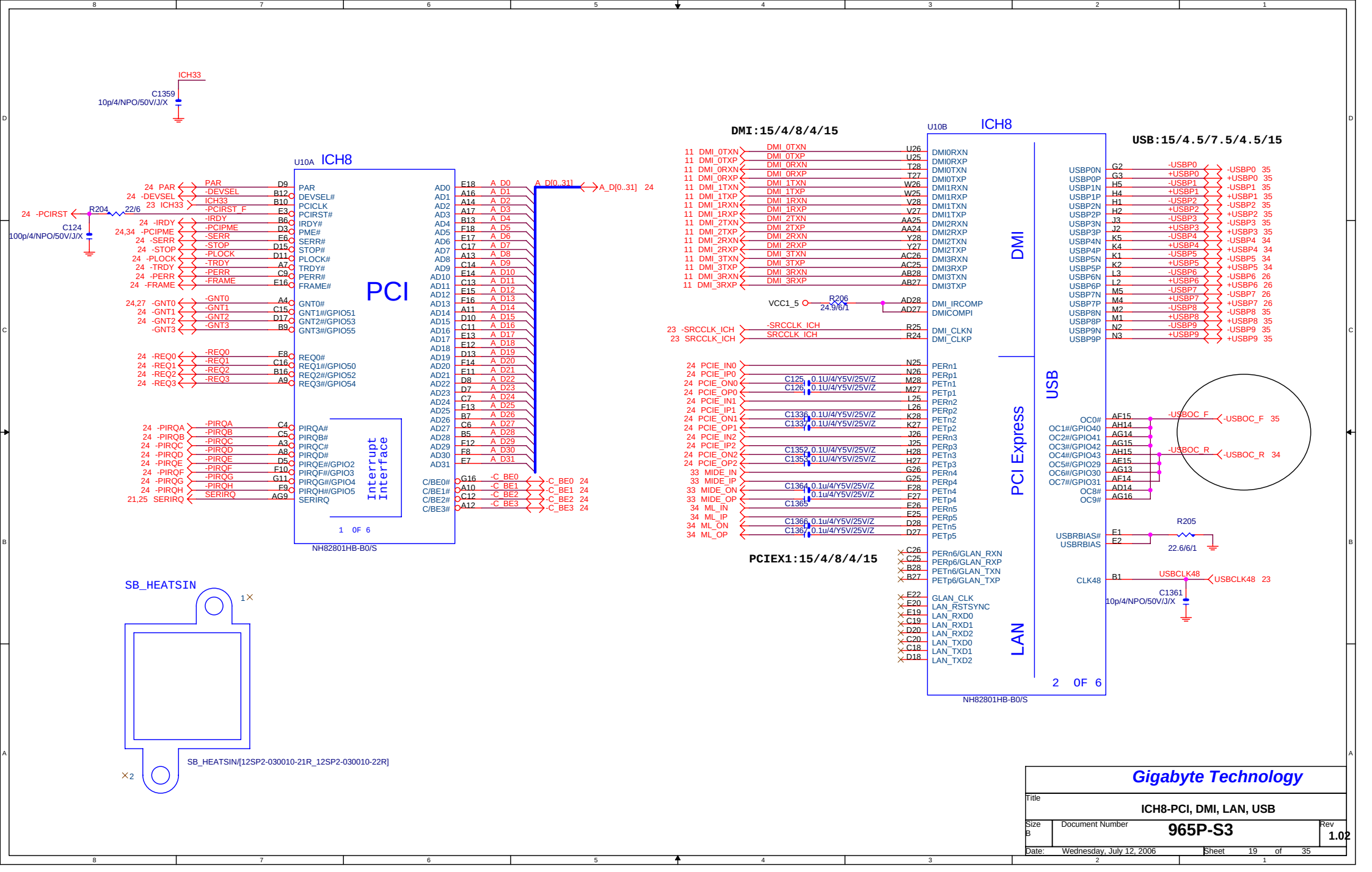

Gigabyte Technology		
Title: ICH8-PCI, DMI, LAN, USB		
Size: B	Document Number: 965P-S3	Rev: 1.02
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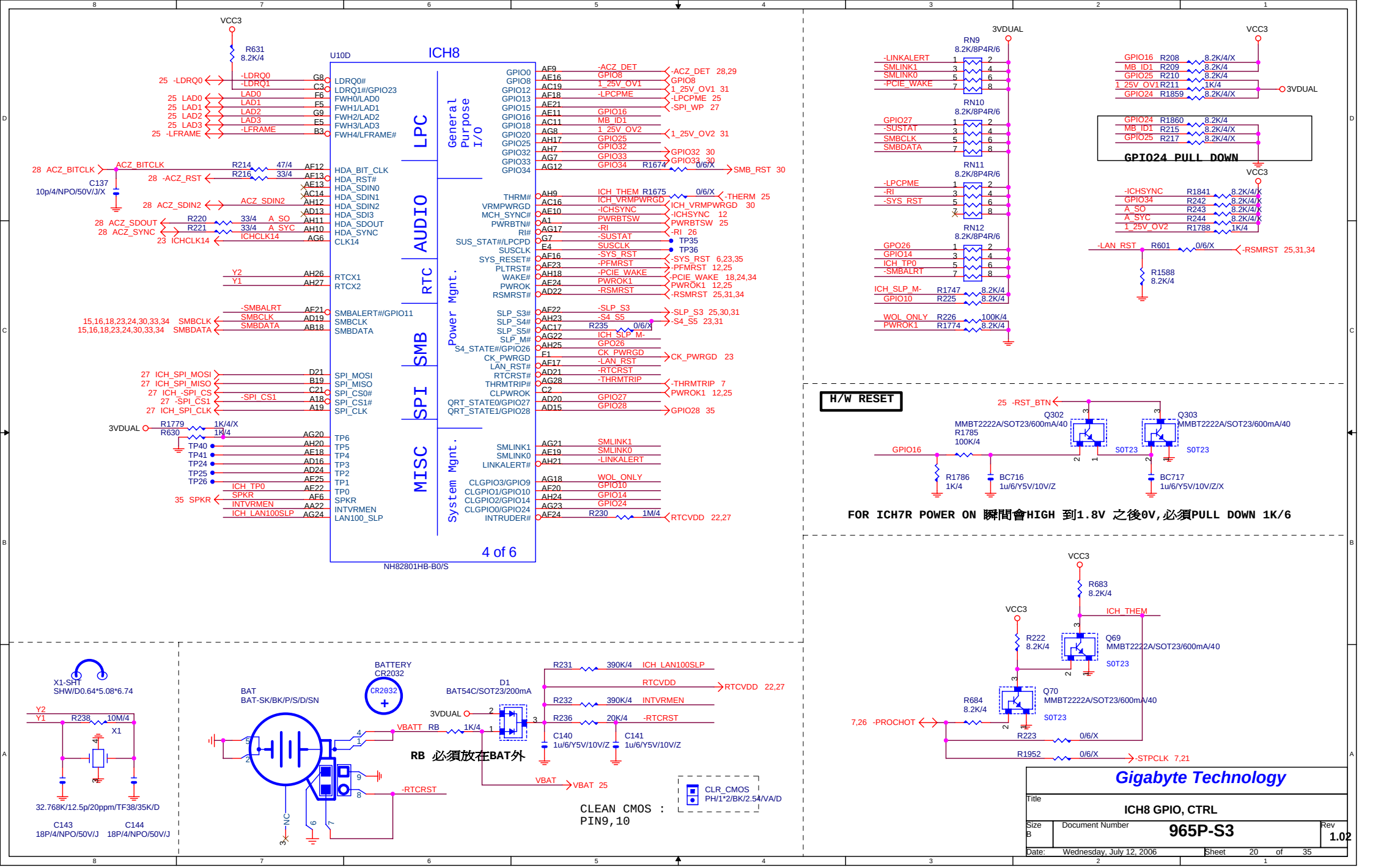
ICH8
U10D
LPC
AUDIO
RTC
SMB
SPI
MISC
General Purpose I/O
Power Mgnt.
System Mgnt.
LDRQ0#
LDRQ1#/GPIO23
FWH0/LAD0
FWH1/LAD1
FWH2/LAD2
FWH3/LAD3
FWH4/LFRAME#
HDA_BIT_CLK
HDA_RST#
HDA_SDIN0
HDA_SDIN1
HDA_SDIN2
HDA_SDI3
HDA_SDOUT
HDA_SYNC
CLK14
RTCX1
RTCX2
SMBALERT#/GPIO11
SMBCLK
SMBDATA
SPI_MOSI
SPI_MISO
SPI_CS0#
SPI_CS1#
SPI_CLK
TP6
TP5
TP4
TP3
TP2
TP1
TP0
SPKR
INTVRMEN
LAN100_SLP
4 of 6
NH82801HB-B0/S
3VDUAL
RN9
RN10
RN11
RN12
8.2K/8P4R/6
GPIO24 PULL DOWN
H/W RESET
FOR ICH7R POWER ON 瞬間會HIGH 到1.8V 之後0V,必須PULL DOWN 1K/6
Q302
Q303
MMBT2222A/SOT23/600mA/40
Q69
Q70
BATTERY
CR2032
BAT
BAT-SK/BK/P/S/D/SN
D1
BAT54C/SOT23/200mA
RB 必須放在BAT外
CLEAN CMOS :
PIN9,10
CLR_CMOS
PH/1*2/BK/2.54/VA/D
X1-SHT
SHW/D0.64*5.08*6.74
X1
32.768K/12.5p/20ppm/TF38/35K/D
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ICH8 GPIO, CTRL
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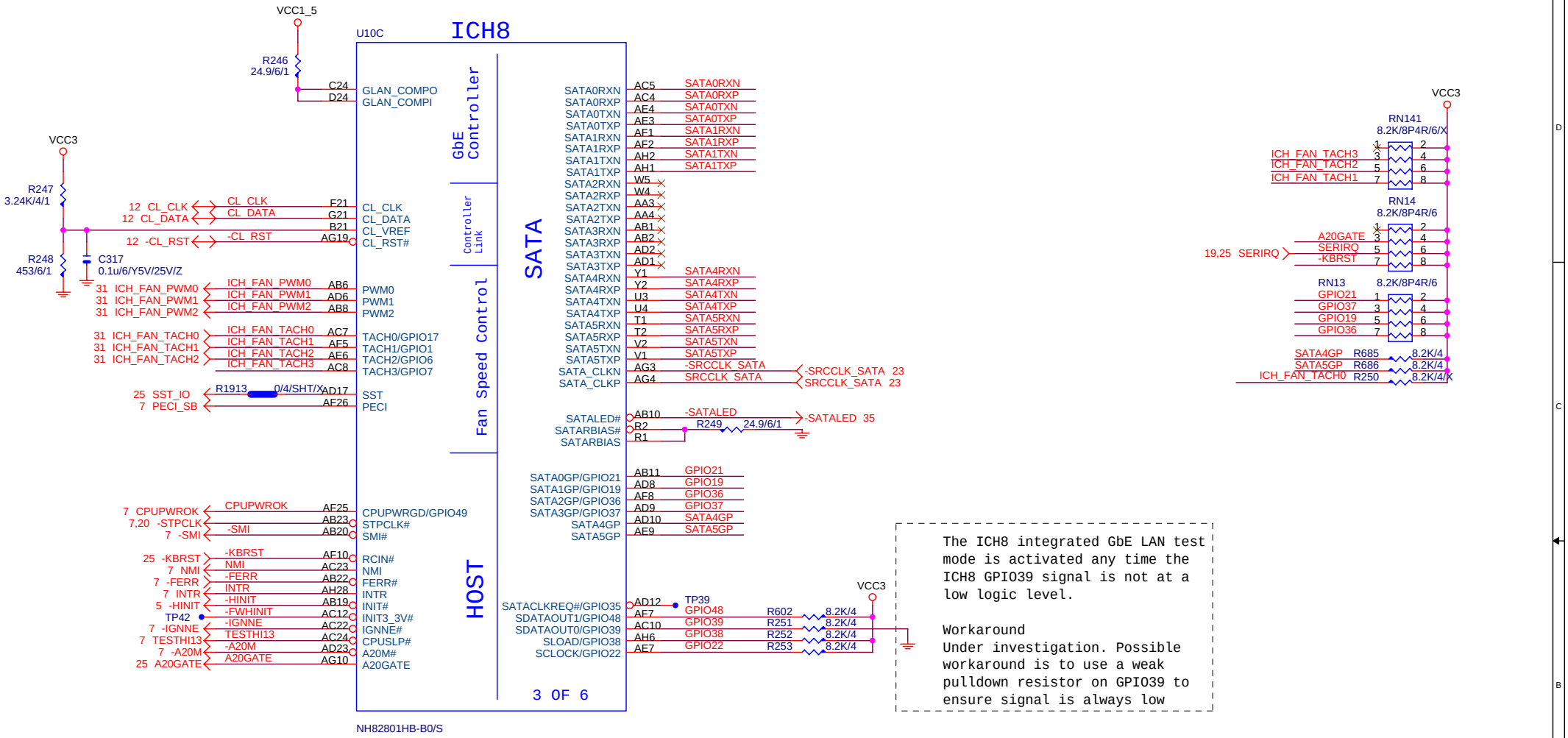

Gigabyte Technology			
Title: ICH6- SATA, FAN CTRL			
Size: Custom	Document Number: 965P-S3		Rev: 1.02
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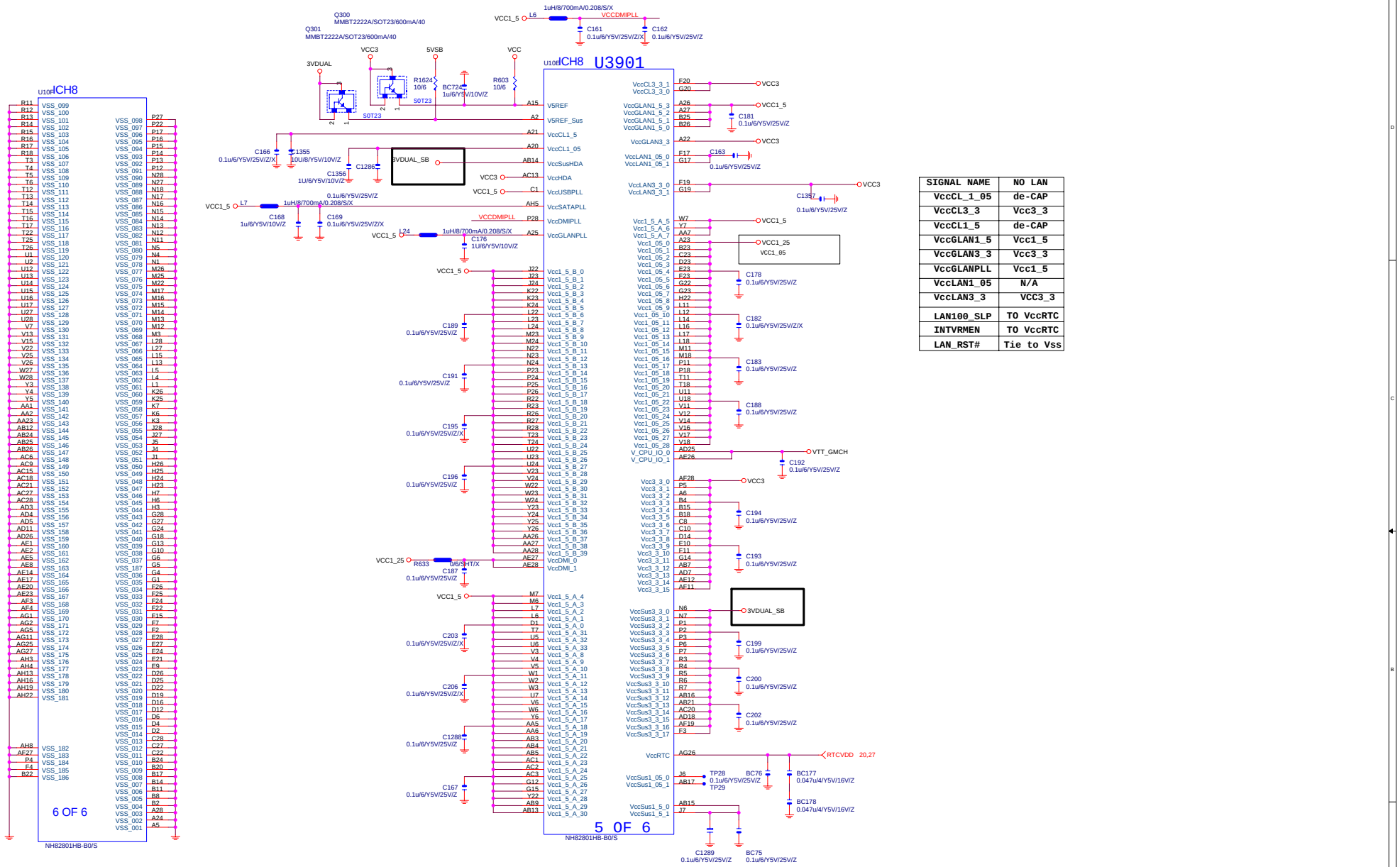

SIGNAL NAME	NO LAN
VccCL_1_05	de-CAP
VccCL3_3	Vcc3_3
VccCL1_5	de-CAP
VccGLAN1_5	Vcc1_5
VccGLAN3_3	Vcc3_3
VccGLANPLL	Vcc1_5
VccLAN1_05	N/A
VccLAN3_3	VCC3_3
LAN100_SLP	TO VccRTC
INTVRMEN	TO VccRTC
LAN_RST#	Tie to Vss

Gigabyte Technology			
Title: ICH6-PWR & GND			
Size: C	Document Number: 965P-S3		Rev: 1.02
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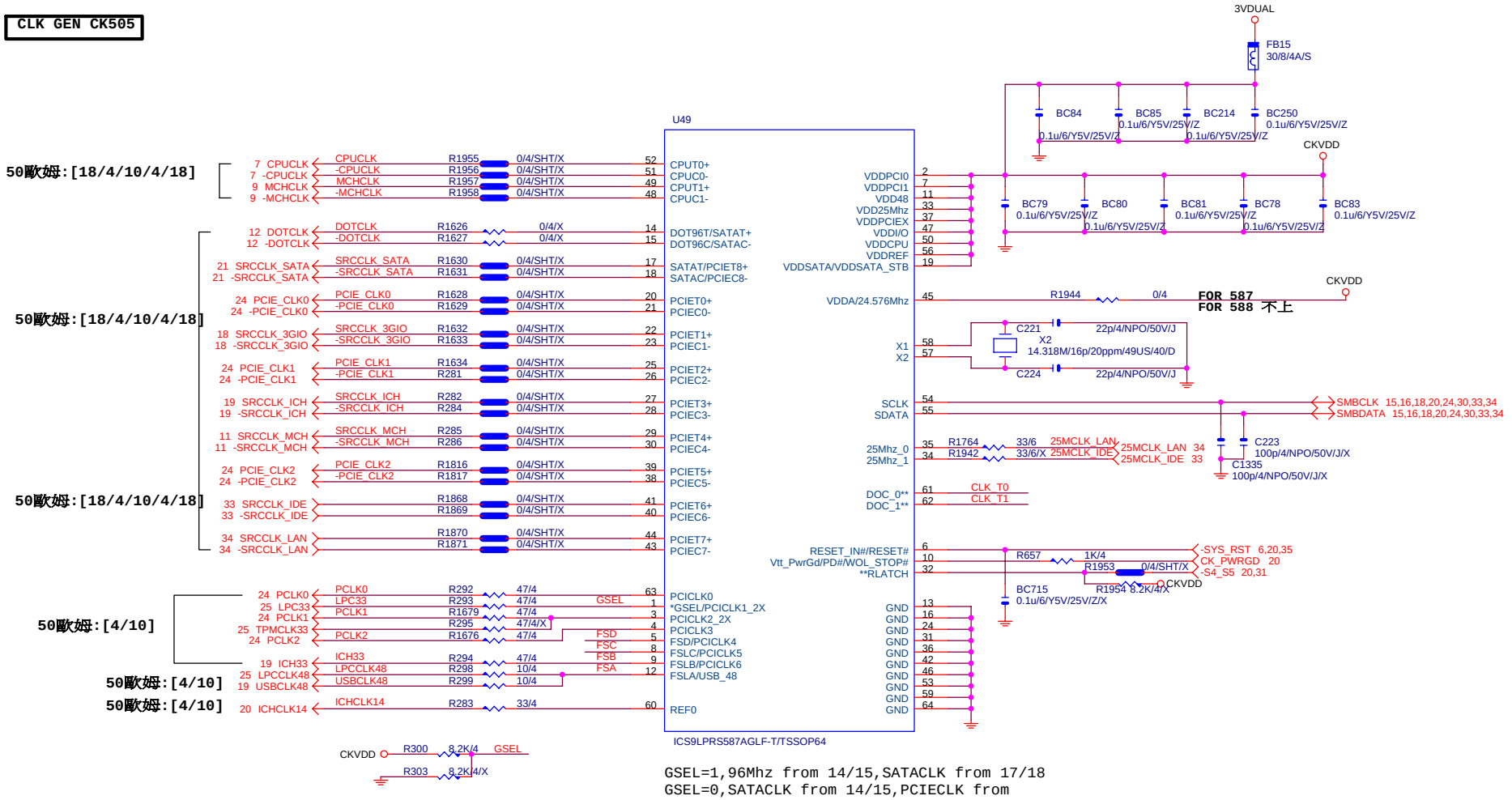
CLK GEN CK505



Title	CK505 CLK GEN
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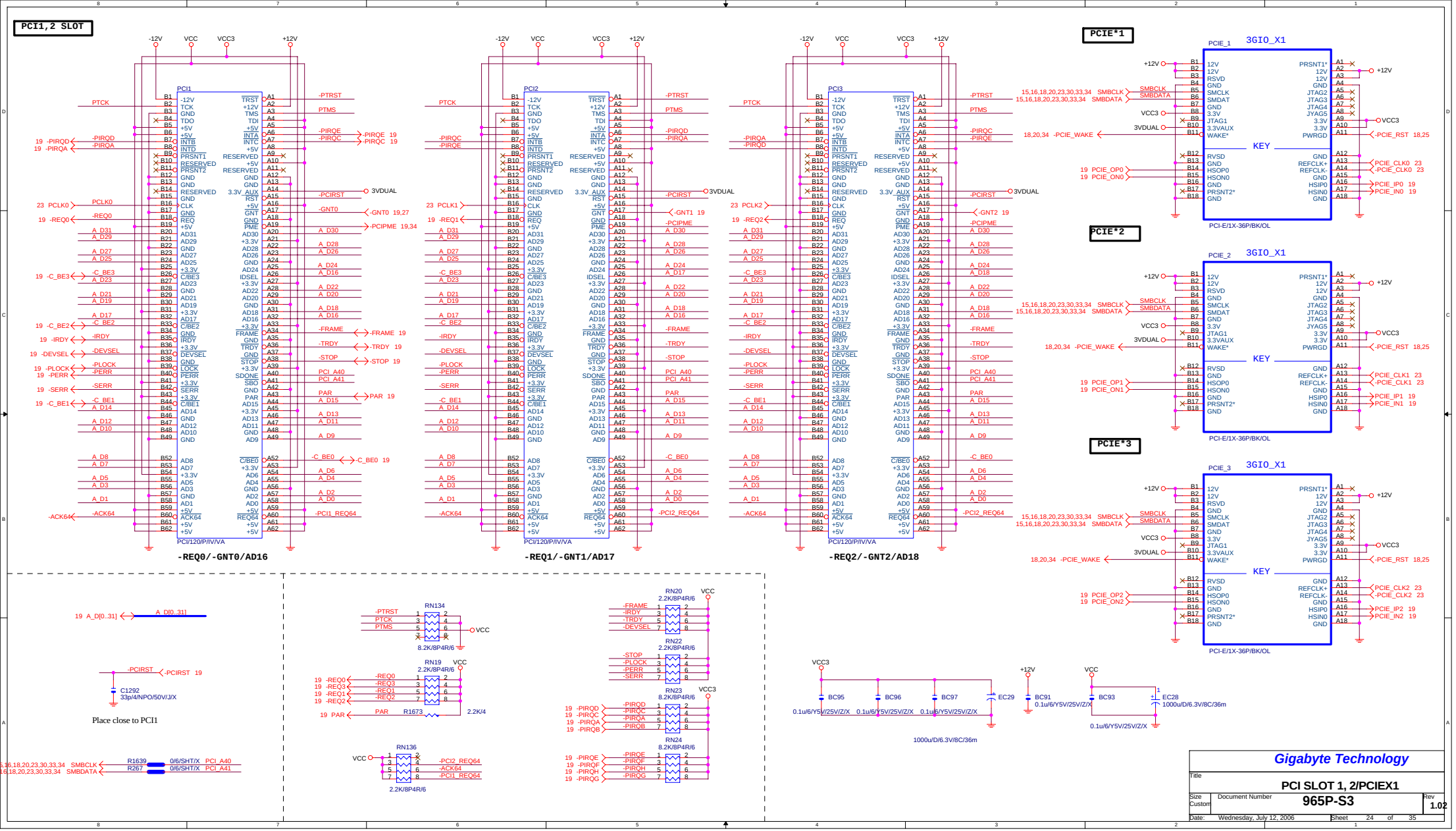
PCI1,2 SLOT
PCI1
PCI2
PCI3
PCI120/P/IV/VA
-REQ0/-GNT0/AD16
-REQ1/-GNT1/AD17
-REQ2/-GNT2/AD18
PCIE*1
PCIE*2
PCIE*3
PCIE_1
PCIE_2
PCIE_3
3GIO_X1
KEY
PCI-E/1X-36P/BK/OL
Place close to PCI1
C1292
33p/4/NPO/50V/J/X
R1639
R267
0/6/SHT/X
RN134
RN19
RN20
RN22
RN23
RN24
RN136
2.2K/8P4R/6
8.2K/8P4R/6
R1673
2.2K/4
BC95
BC96
BC97
EC29
BC91
BC93
EC28
0.1u/6/Y5V/25V/Z/X
1000u/D/6.3V/8C/36m
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PCI SLOT 1, 2/PCIEX1
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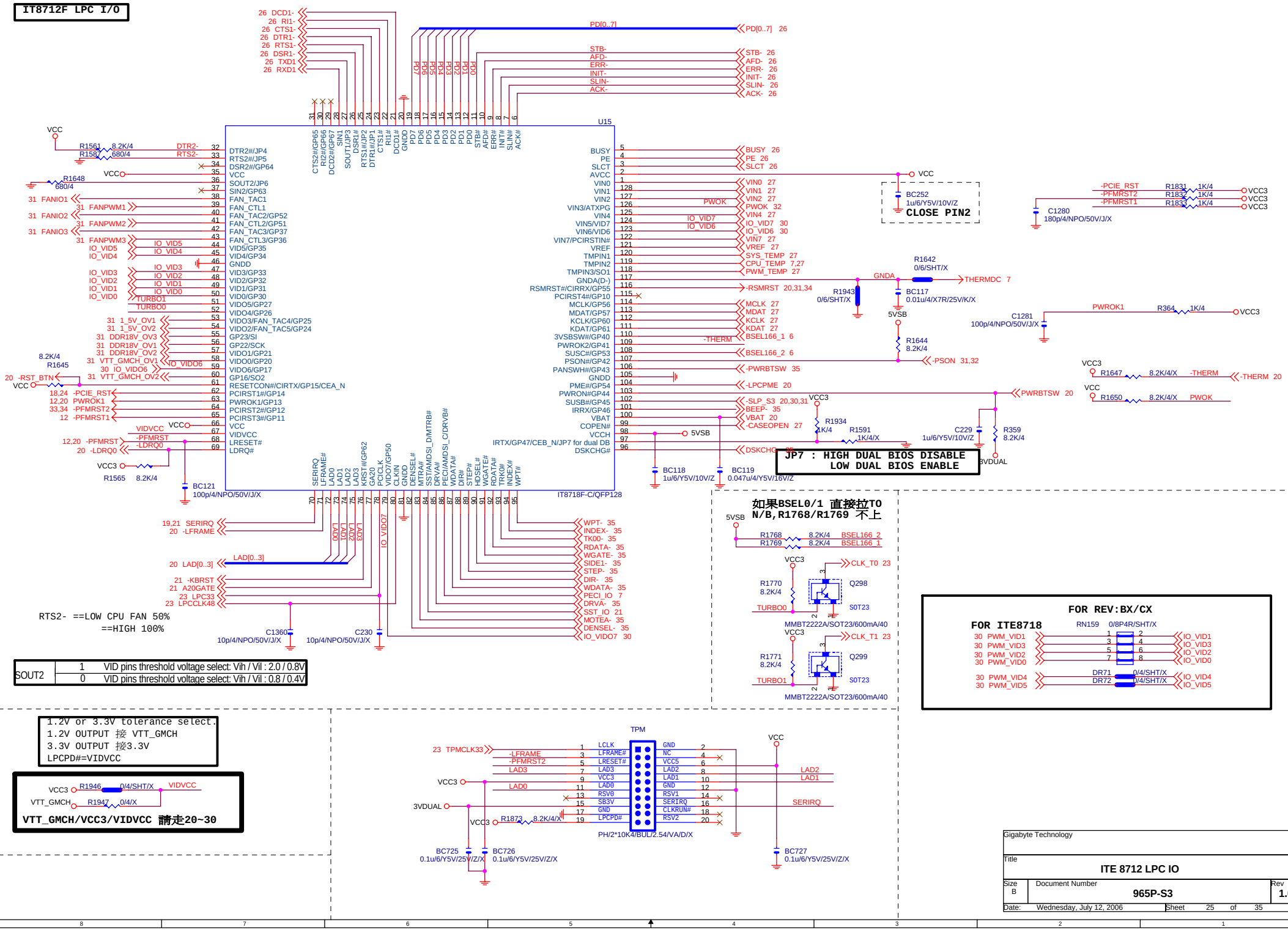
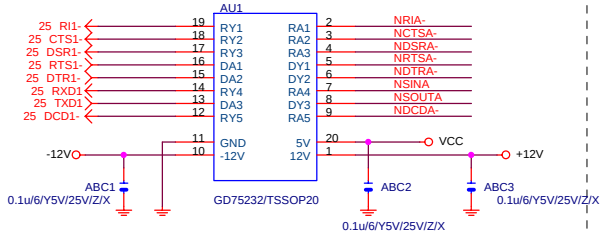
IT8712F LPC I/O

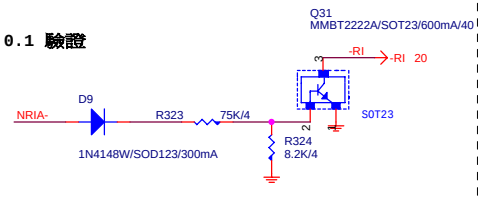


COMA

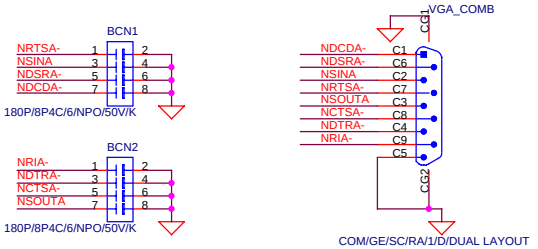


COM RI

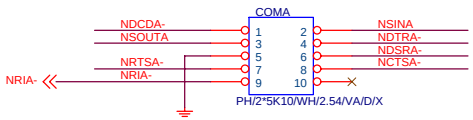
REV:0.1 驗證

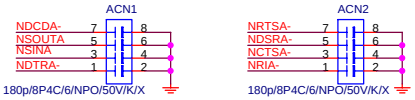


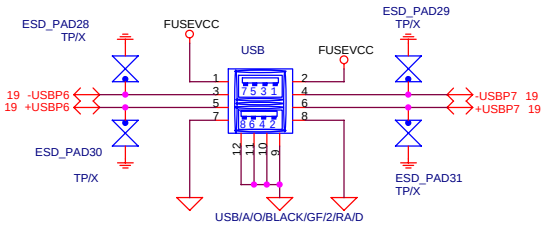
EXTERNAL COMB



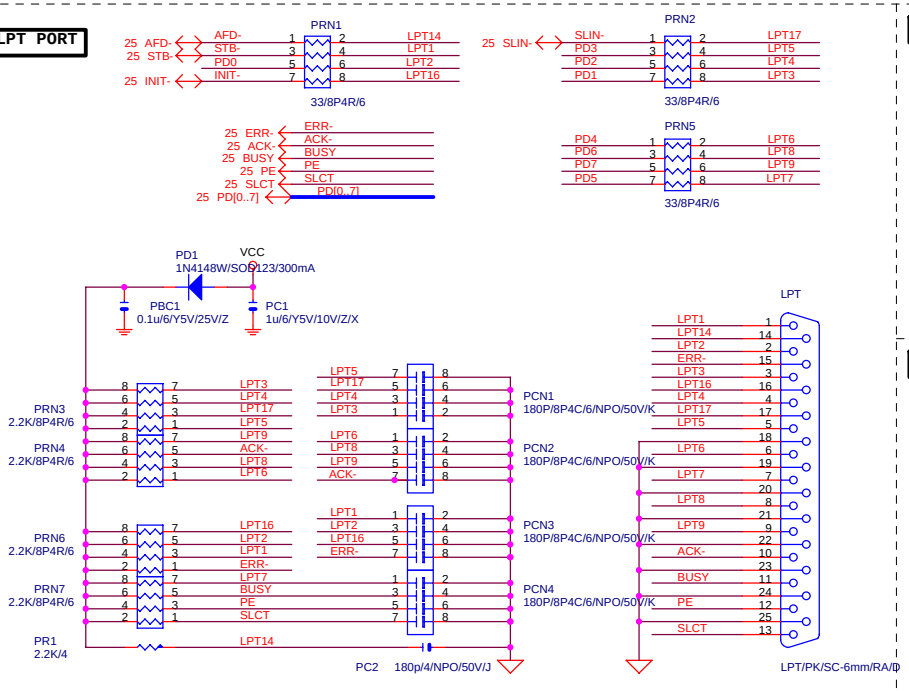
PLACE NEAR VGA_COM CONNECTOR



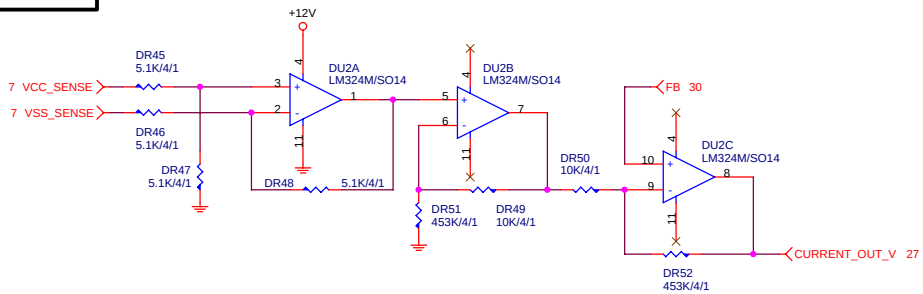




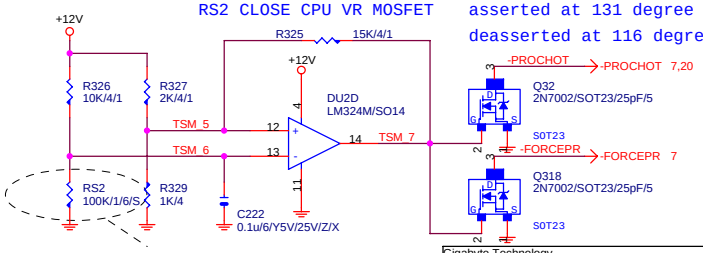
LPT PORT



DYNAMIC CURRENT OC



-PROHOT



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Title: COM & LPT PORT

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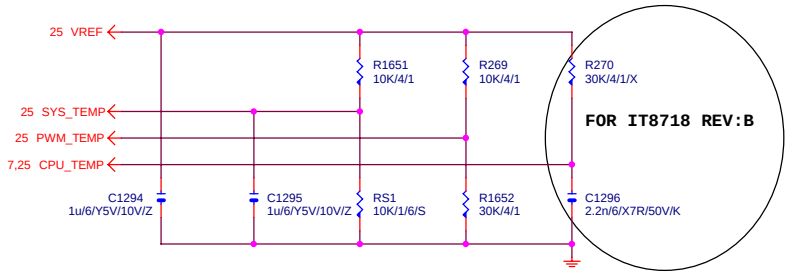
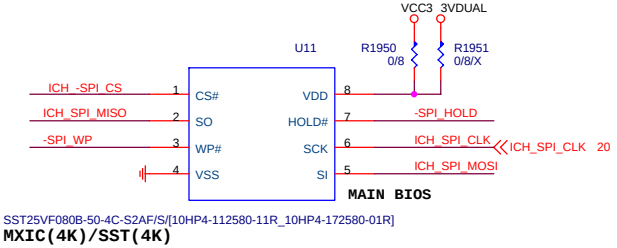
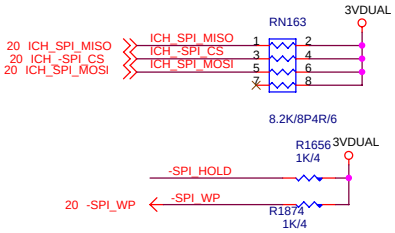
TEMP H/W MONITOR





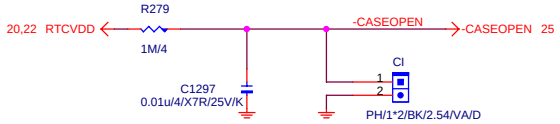
SST25VF080B-50-4C-S2AF/S/[10HP4-112580-11R_10HP4-172580-01R]

MXIC(4K)/SST(4K)

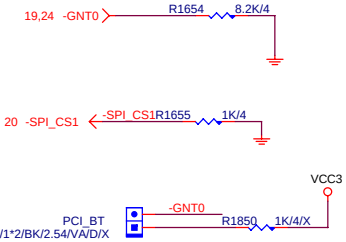


BOOT DEVICE	GNT0	CS1
SPI	0	X
PCI	1	0
FWH	1	1

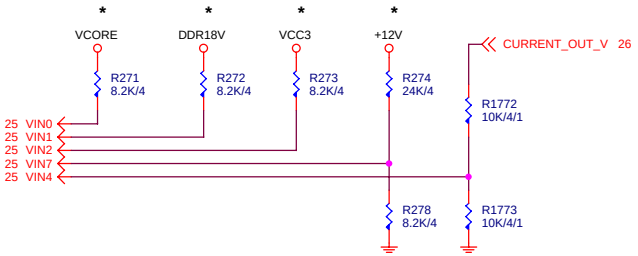
CASE OPEN

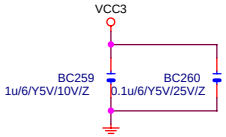


Case Open Circuits

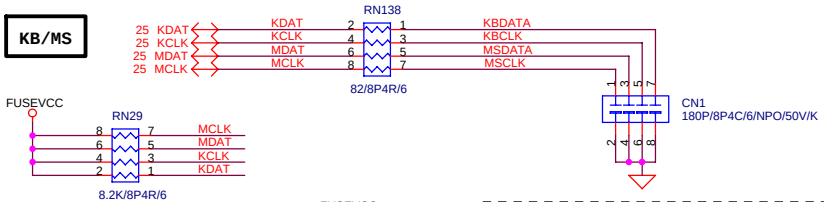


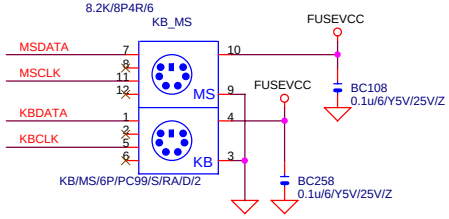
VOLTAGE-- H/W MONITOR

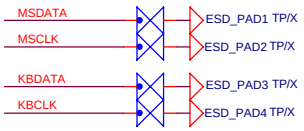




KB/MS







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Title: **BIOS/HW-MONITOR/CI/KB/MS**

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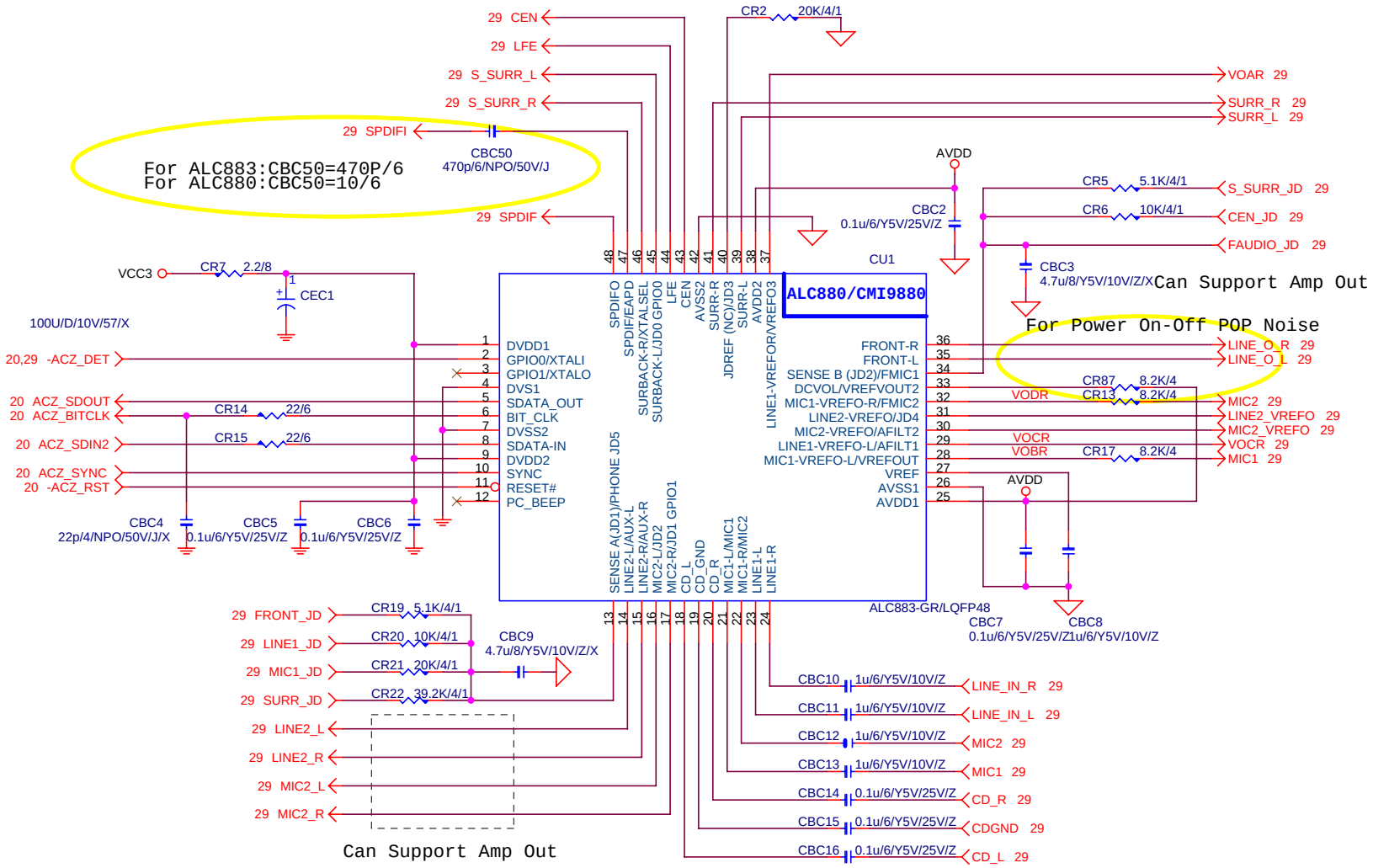
AZALIA CODEC



Gigabyte Technology		
Title: AC97 ALC658		
Size: Custom	Document Number: 965P-S3	Rev: 1.02
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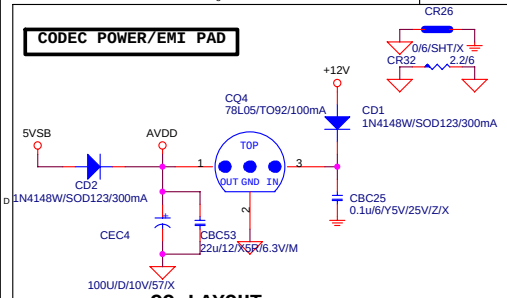
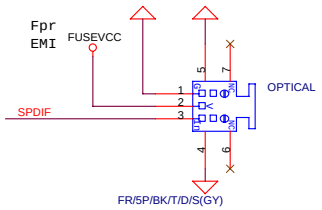
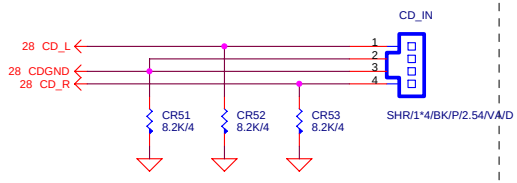
CODEC POWER/EMI PAD

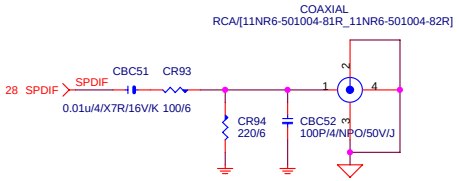


CO-LAYOUT

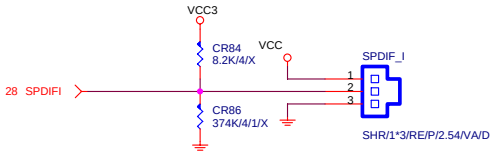


CD IN

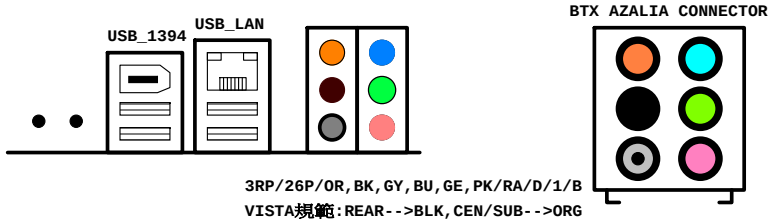


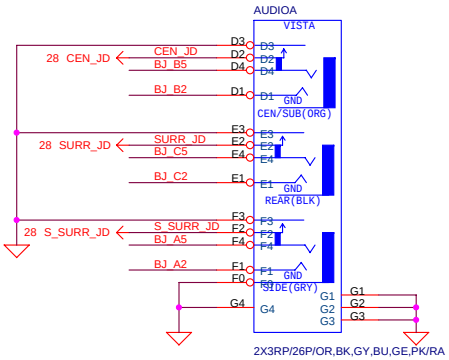


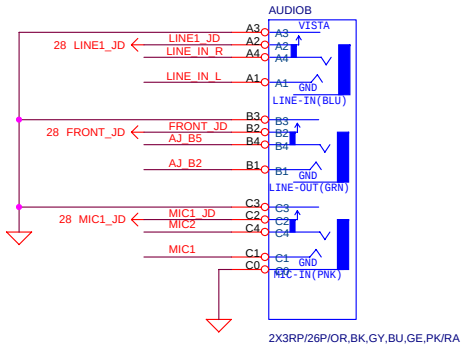
SPDIF



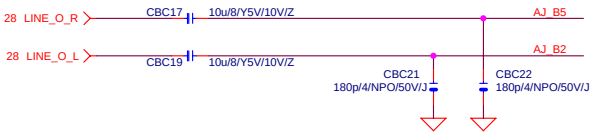
AZALIA JACK



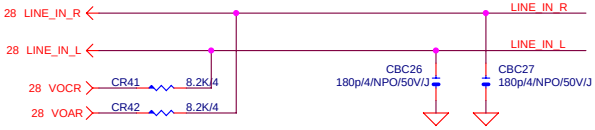




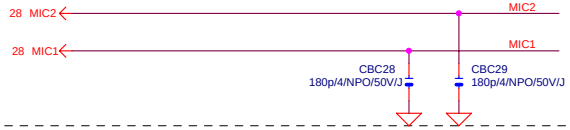
LINE-OUT



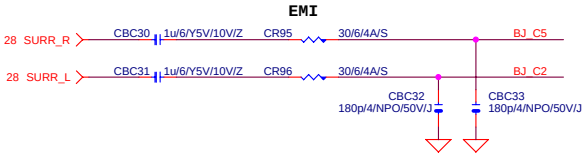
LINE-IN



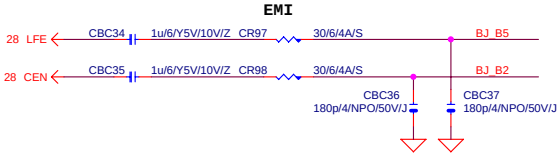
MIC-IN



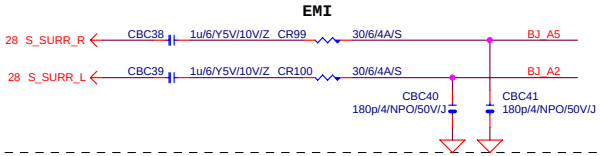
SURROUND



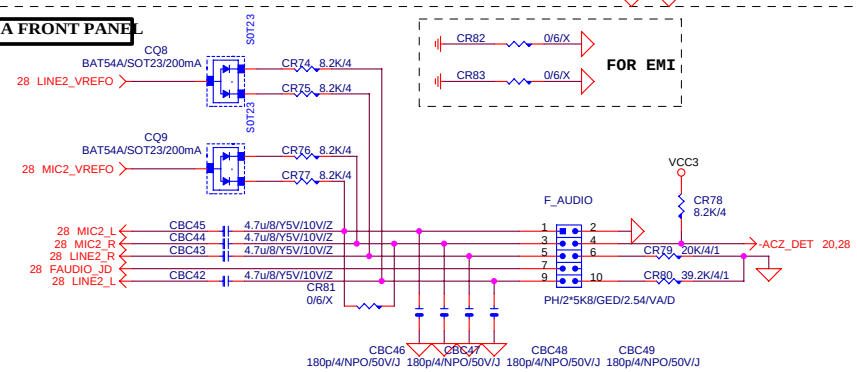
CEN/LFE



SURR BACK



AZALIA FRONT PANEL

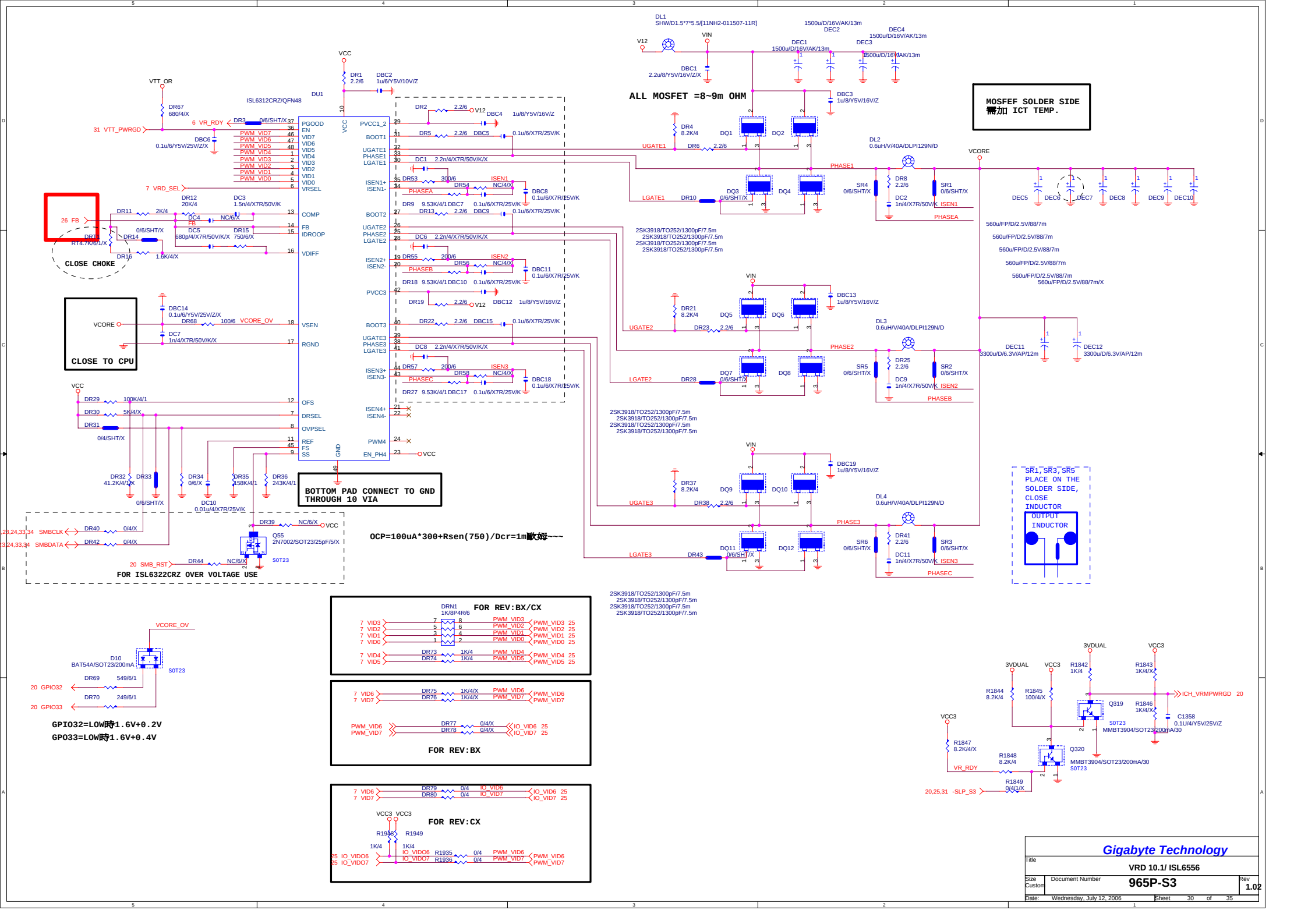


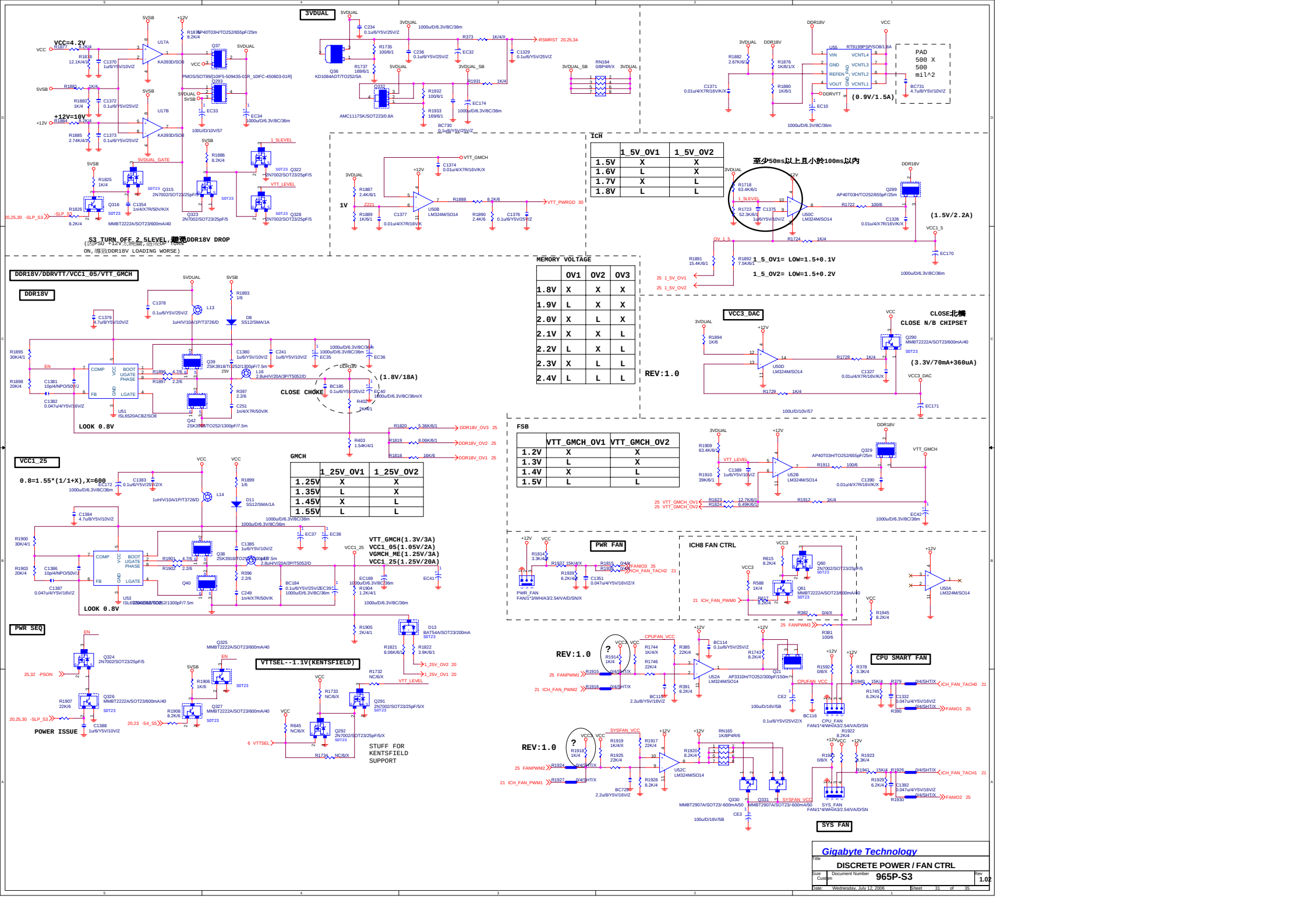
Gigabyte Technology

Title: AUDIO JACK

Size: Custom | Document Number: 965P-S3 | Rev: 1.02

Date: Wednesday, July 12, 2006 | Sheet 29 of 35


ALL MOSFET =8~9m OHM
MOSFEF SOLDER SIDE
需加 ICT TEMP.
CLOSE CHOKE
CLOSE TO CPU
BOTTOM PAD CONNECT TO GND
THROUGH 10 VIA
FOR ISL6322CRZ OVER VOLTAGE USE
OCP=100uA*300+Rsen(750)/Dcr=1m歐姆~~~
SR1,SR3,SR5
PLACE ON THE
SOLDER SIDE,
CLOSE
INDUCTOR
OUTPUT
INDUCTOR
FOR REV:BX/CX
FOR REV:BX
FOR REV:CX
GPIO32=LOW時1.6V+0.2V
GPO33=LOW時1.6V+0.4V
ISL6312CRZ/QFN48
2SK3918/TO252/1300pF/7.5m
560u/FP/D/2.5V/88/7m
3300u/D/6.3V/AP/12m
MMBT3904/SOT23/200mA/30
Gigabyte Technology
VRD 10.1/ ISL6556
965P-S3
1.02
Wednesday, July 12, 2006



	1_5V_0V1	1_5V_0V2
1.5V	X	X
1.6V	L	X
1.7V	X	L
1.8V	L	L

	0V1	0V2	0V3
1.8V	X	X	X
1.9V	L	X	X
2.0V	X	L	X
2.1V	X	X	L
2.2V	L	X	L
2.3V	X	L	L
2.4V	L	L	L

	VTT_GMCH_OV1	VTT_GMCH_OV2
1.2V	X	X
1.3V	L	X
1.4V	X	L
1.5V	L	L

	1_25V_0V1	1_25V_0V2
1.25V	X	X
1.35V	L	X
1.45V	X	L
1.55V	L	L

Gigabyte Technology		
Title: DISCRETE POWER / FAN CTRL		
Size: Custom	Document Number: 965P-S3	Rev: 1.02
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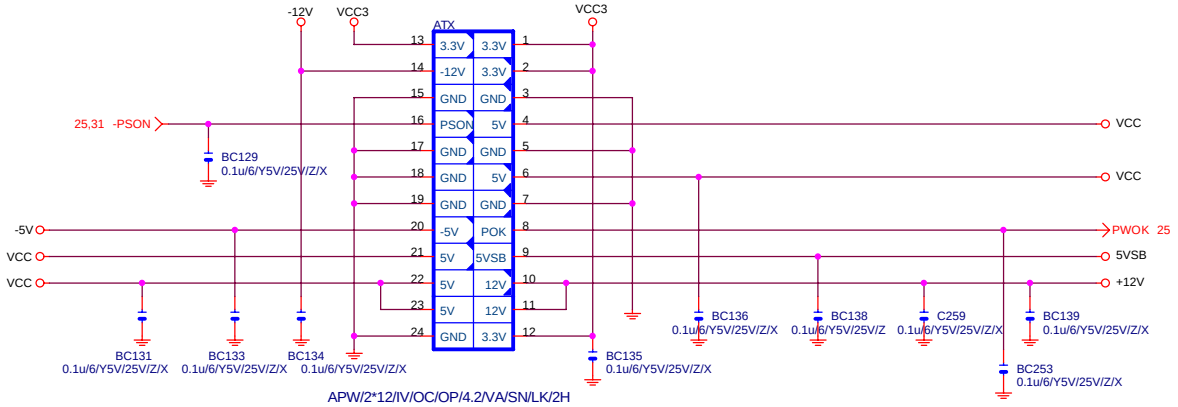
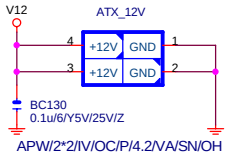
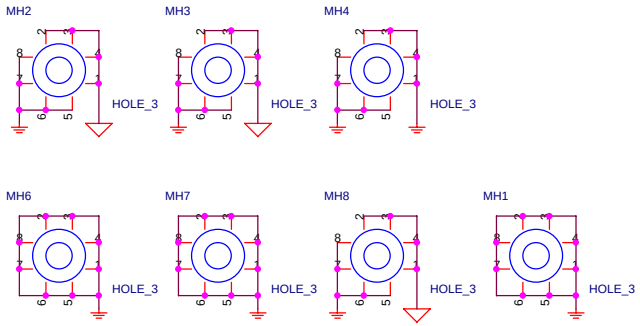
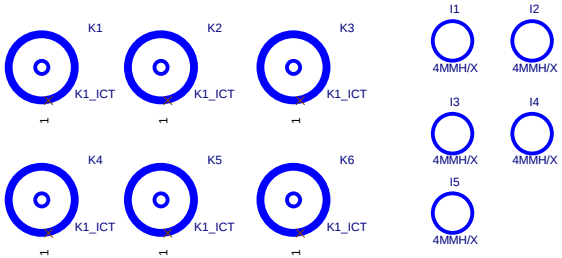
ATX POWER CONNECTOR





HOLE_3-2--->有鉛





Gigabyte Technology		
Title: ATX POWER CONNECTOR		
Size: B	Document Number: 965P-S3	Rev: 1.02
Date: Wednesday, July 12, 2006	Sheet 32 of 35	

3.3V to 1.8V Voltage Regulator

AMC1117SK/SOT223/0.8A

RQ1

VCC_1.8V

VCC3

RR21 100/4/1

RR22 44.2/4/1

REC1

RBC1 0.1u/4/Y5V/16V/Z

RBC2 10u/8/Y5V/10V/Z

100U/D/10V/57

JMB363

LQFP 100 14x14

JMicron

RU1

GBB363/3

VCC3

RBC3 RBC4 RBC5 RBC6 RBC7 RBC8 RBC9

0.1u/4/Y5V/16V/Z

10u/8/Y5V/10V/Z

close to IC

25,34 -PFMRST2

RC3 100P/4/N/50V/X

VCC3

RBC10 10u/8/Y5V/10V/Z

RBC11 0.1u/4/Y5V/16V/Z

RBC12 0.1u/4/Y5V/16V/Z

REC2

RBC13 0.1u/4/Y5V/16V/Z

Close to pin42 and pin53

100U/D/10V/57

VCC_1.8V DVDD_1.8V

RBC14 RBC15 RBC16 RBC17 RBC18

0.1u/4/Y5V/16V/Z

10u/8/Y5V/10V/Z

close to IC

VCC_1.8V ASVDD_1.8V

RBC19 RBC20 RBC21

RBC22 RBC23 RBC24

0.1u/4/Y5V/16V/Z

10u/8/Y5V/10V/Z

Close to pin58

Close to pin47

VCC_1.8V APVDD_1.8V

RBC25 RBC26

RBC27 RBC28 RBC29

0.1u/4/Y5V/16V/Z

10u/8/Y5V/10V/Z

1n/4/X7R/50V/K

CLOSE TO pin22

close to pin17

3VDUAL

RR39 820/6/1/X 1.85V

RR41 1K/6/1/X

+12V

U52D LM324M/SO14

RR40 1K/4/X

RR42 1K/4/X

RQ4 2N7002/SOT23/25pF/5/X SOT23

RQ5 2N7002/SOT23/25pF/5/X SOT23

VCC_1.8V

RC5 RC6 0.1u/4/Y5V/16V/Z

MIDE_IP 19

MIDE_IN 19

MIDE_ON 19

MIDE_OP 19

SRCCLK_IDE 23

-SRCCLK_IDE 23

PCIE_REXT SATA_REXT1 SATA_REXT0

RR31 12K/4/1 RR32 12K/4/1 RR33 12K/4/1

Near to PIN

PH_IORDY RR29 1K/4

CSELA RR30 0/4

PH_DMARQ RR34 8.2K/4

PH_INTRQ RR35 8.2K/4

DD7A RR36 8.2K/4

VCC3

RR19 0/6/X 25MCLK_IDE 23

會漏電

XTALI XTALO

RC1 33P/4/NPO/50V/J

RR20 1M/4

RX1 25M/20p/30ppm/49USX/20/D

RC2 33P/4/NPO/50V/J

RR23 8.2K/4 RR24 8.2K/4

SMB_CLK SMB_DAT

RR25 0/4/X RR26 0/4/X

SMBCLK 15,16,18,20,23,24,30,34

SMBDATA 15,16,18,20,23,24,30,34

RD1 BAW56/SOT23/300mA

DASPnXA HD_LEDn

MMBT2222A/SOT23/600mA/40

RR27 1K/4

RQ2 SOT23

-HDLED

-HDLED 35

RC4 180P/4/N/50V/X

RR28 0/4/X

SATA Connector

SATA_TXP0 RC7 0.01u/4/X7R/16V/K SATA_RXP1

SATA_TXN0 RC9 0.01u/4/X7R/16V/K SATA_RXN1

SATA_RXN0 RC11 0.01u/4/X7R/16V/K SATA_TXN1

SATA_RXP0 RC13 0.01u/4/X7R/16V/K SATA_TXP1

GSATAII0_1

SATA2/7/PU/H/P/VA/D2/B/GBT

IDE Connector

IDE1

BH/2*20K20/GEL/N/2.54/VA/D/GF

(#20 key-pin)

(#28 CSEL)

(#32 IOCS16)

PH_RESETnA

RR37 1K/4

RR38 8.2K/4

RQ3 MMBT2222A/SOT23/600mA/40 SOT23

RESETnA

PH_DD7 PH_DD8 PH_DD6 PH_DD9 → DD7A DD8A DD6A DD9A

PH_DD5 PH_DD4 PH_DD10 PH_DD11 → DD5A DD4A DD10A DD11A

PH_DD3 PH_DD12 PH_DD2 PH_DD13 → DD3A DD12A DD2A DD13A

PH_DD1 PH_DD0 PH_DD14 PH_DD15 → DD1A DD0A DD14A DD15A

PH_DIOW_N → DIOWnA

PH_DIOR_N → DIORnA

PH_DMACK_N → DMACKnA

PH_DA1 → DA1A

PH_DA0 → DA0A

PH_CS0_N → CS0nA

PH_DA2 → DA2A

PH_CS1_N → CS1nA

PH_IORDY → IORDYA

PH_DMARQ → DMARQA

PH_INTRQ → INTRQA

PH_CBLID_N → PDIAGnA

Gigabyte Technology	
Title	JMR363
Size C	Document Number 965P-S3 Rev 1.02
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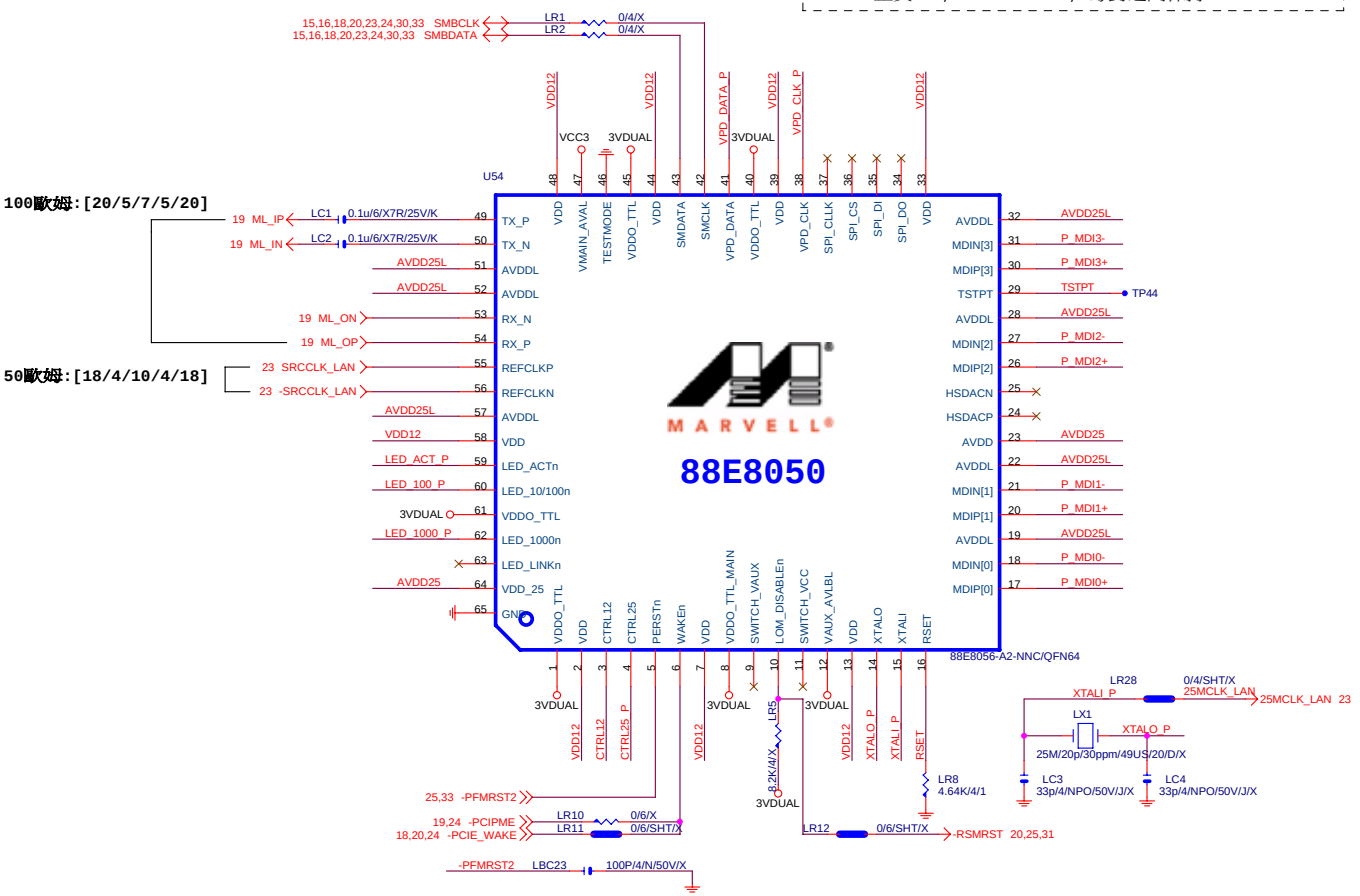
PCIE-1G LAN

 # Layout Check 注意事項

1. LU1 PIN65 需下內層GND,打 12 VIA
2. 3VDUAL , VCC3 , VDD15_L , AVDD25_L
   至少走20mil寬,並且電容擺設每兩pin至少放一顆Bypass Cap.
3. X'TAL 25MHz 兩訊號線,TRACE 愈短愈好,線寬12mil
4. MDI正負0~3,TRACE 8:7:8 , 每對之間保持 40mil

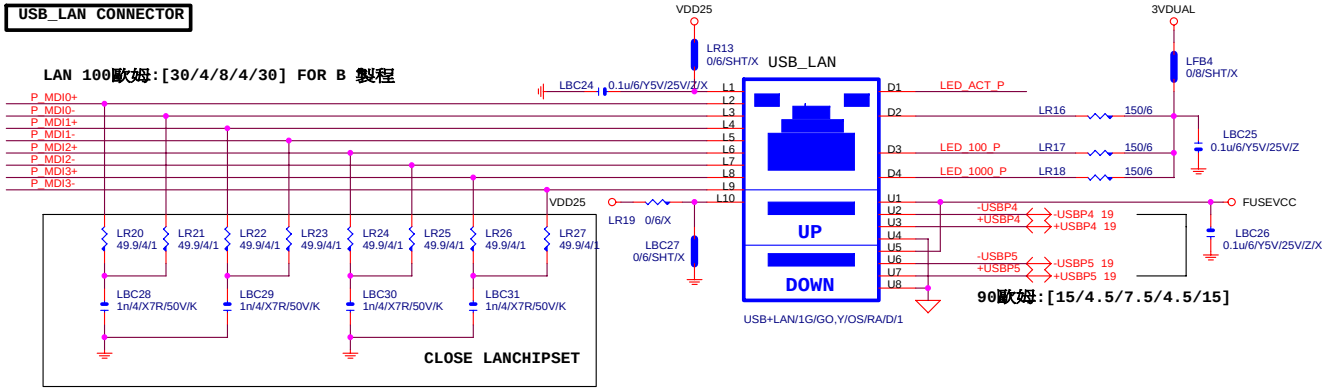
100歐姆:[20/5/7/5/20]

50歐姆:[18/4/10/4/18]

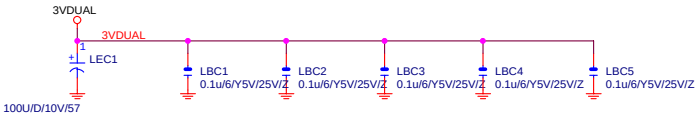


USB_LAN CONNECTOR

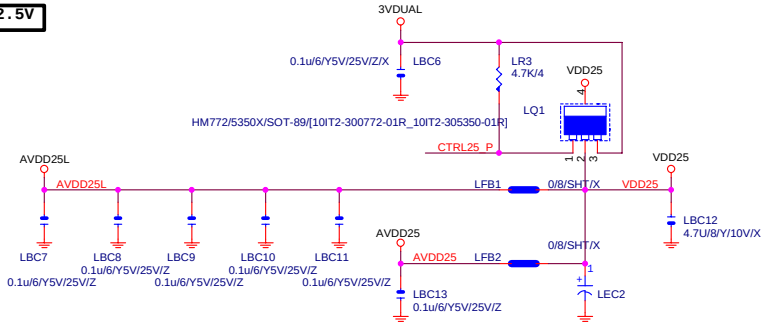
LAN 100歐姆:[30/4/8/4/30] FOR B 製程



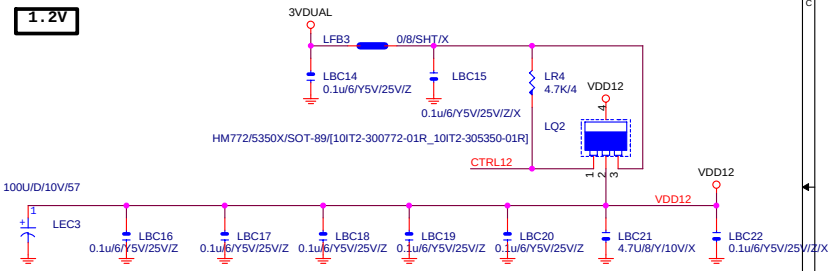
3VDUAL

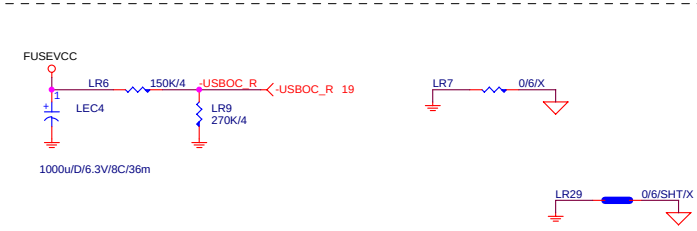


2.5V

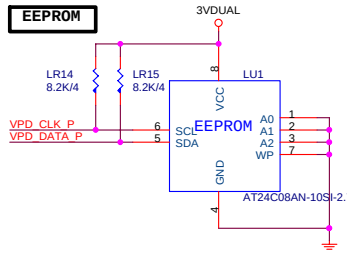


1.2V

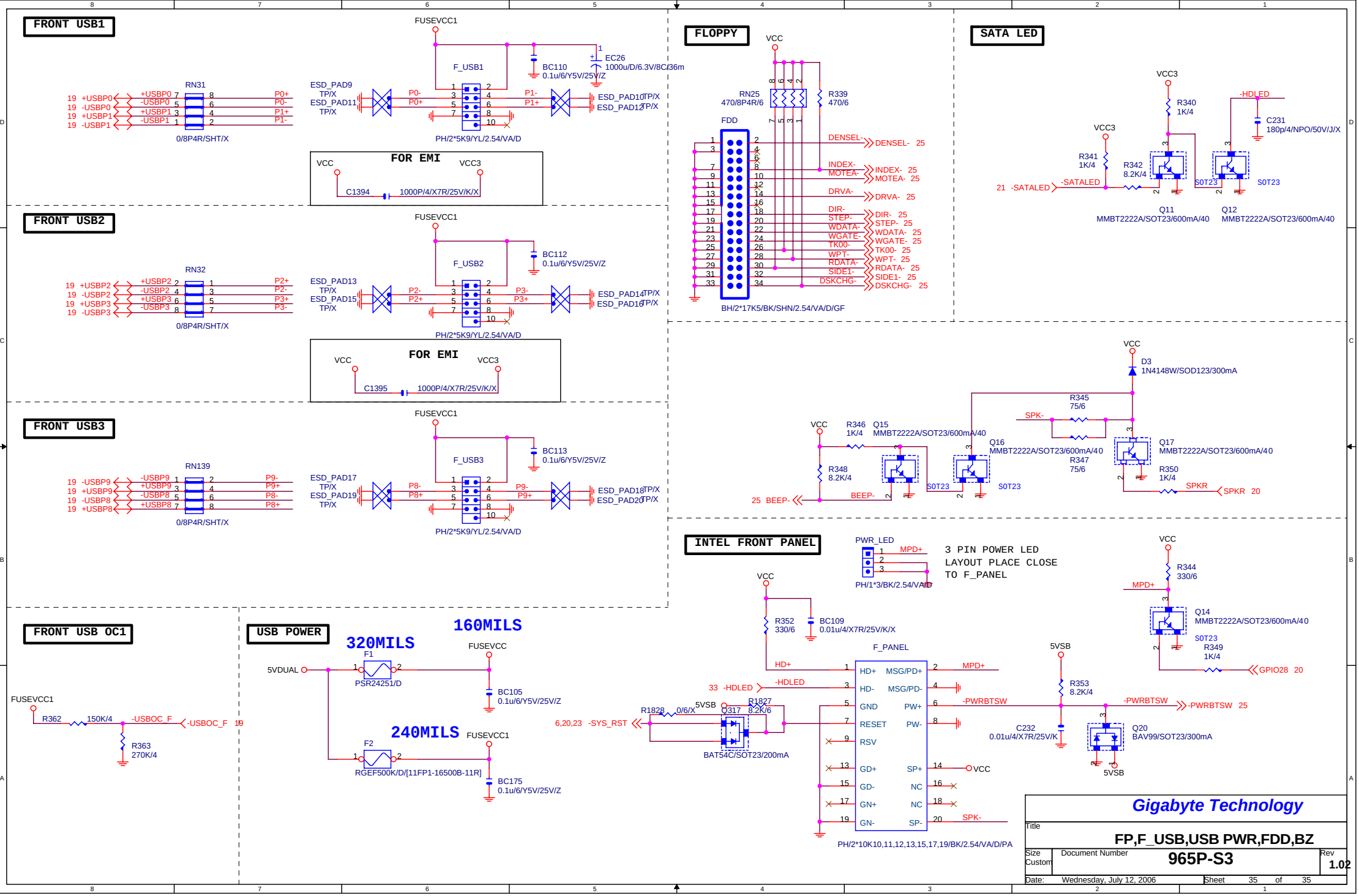




EEPROM



Gigabyte Technology		
Title: MARVELL 88E8001		
Size: Custom	Document Number: 965P-S3	Rev: 1.02
Date: Wednesday, July 12, 2006	Sheet 34 of 35	


FRONT USB1
RN31
0/8P4R/SHT/X
FUSEVCC1
F_USB1
PH/2*5K9/YL/2.54/VA/D
FOR EMI
C1394
1000P/4/X7R/25V/K/X
FRONT USB2
RN32
F_USB2
C1395
FRONT USB3
RN139
F_USB3
FRONT USB OC1
R362
150K/4
R363
270K/4
USB POWER
320MILS
160MILS
240MILS
PSR24251/D
RGEF500K/D/[11FP1-16500B-11R]
FLOPPY
RN25
470/8P4R/6
R339
470/6
FDD
BH/2*17K5/BK/SHN/2.54/VA/D/GF
SATA LED
R340
1K/4
R341
1K/4
R342
8.2K/4
C231
180p/4/NPO/50V/J/X
Q11
MMBT2222A/SOT23/600mA/40
Q12
MMBT2222A/SOT23/600mA/40
D3
1N4148W/SOD123/300mA
R345
75/6
R346
1K/4
Q15
R348
8.2K/4
Q16
R347
75/6
Q17
R350
1K/4
INTEL FRONT PANEL
PWR_LED
PH/1*3/BK/2.54/VA/D
3 PIN POWER LED
LAYOUT PLACE CLOSE
TO F_PANEL
R352
330/6
BC109
0.01u/4/X7R/25V/K/X
F_PANEL
PH/2*10K10,11,12,13,15,17,19/BK/2.54/VA/D/PA
R1828
0/6/X
R1827
8.2K/6
Q317
BAT54C/SOT23/200mA
R344
330/6
Q14
R349
1K/4
R353
8.2K/4
C232
0.01u/4/X7R/25V/K
Q20
BAV99/SOT23/300mA
Gigabyte Technology
FP,F_USB,USB PWR,FDD,BZ
965P-S3
1.02
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